XILINX-SYM

IP Interface Connector

IP-Connector

P1

FPGA Configuration

IP_Interface

U2

User Specific I/O

IP - I/O - Connector

IP-Connector

P2

U3

XC17S40L

U7

SN74ALS1034

U5 / U6

EPA424-100

U8

MAX902CSD

U9 / U10 / U11

SN74BCT2545DW

U4

LP3875ES-3.3

U1

SG-8002JF-PTB 9MHZ

H1

HIO7 HIO6 HIO5 HIO4 HIO3 HIO2 HIO1 HIO0

HIO5 is connected to the INIT pin of the XILINX, therefor it cannot be used with jumpers, because then the configuration is not loaded from the PROM!
(should be corrected with a new PCB design)
Reminder: HIO connection in the actual PCB design is missing, a wire must be soldered.

DESY Zeuthen	IP-UNI-XILINX_REV1 Universal I/O Module		
Drawing	F.TONISCH	Date: 9-24-2007_18:14	Sheet: 1 of 1
Design	F.TONISCH		

XCS40XL-4PQ208C

U2

1	GND		
2	GCK1 -I/O	EXT_CLK	
3	I/O	READTP	
4	I/O		
5	I/O	ACK	
6	TDI -I/O		
7	TCK -I/O		
8	I/O	D12	
9	I/O	D13	
10	I/O		
11	I/O		
12	I/O		
13	GND		
14	I/O	D15	
15	I/O	D14	
16	TMS -I/O	D11	
17	I/O	D10	
18	VCC	+3.3V	
19	I/O		
20	I/O	INTREQ1	
21	I/O		
22	I/O		
23	I/O	D8	
24	I/O	D9	
25	GND		
26	VCC	+3.3V	
27	I/O	INTREQ0	
28	I/O		
29	I/O	D7	
30	I/O	D6	
31	I/O	D4	
32	I/O	D5	
33	VCC	+3.3V	
34	I/O	D2	
35	I/O	D3	
36	I/O	D0	
37	I/O	D1	
38	GND		
39	I/O		
40	I/O		
41	I/O		
42	I/O		
43	I/O		
44	I/O		
45	I/O		
46	I/O		
47	I/O		
48	I/O		
49	GCK2 -I/O	IPCLK	
50	M1		
51	GND		
52	M0		

53	VCC	+3.3V	
54	PWRDWN		
55	GCK3 -I/O		
56	HDC		
57	I/O		
58	I/O	HIO0	
59	I/O	HIO1	
60	LDC -I/O	PROM_OE	
61	I/O	HIO2	
62	I/O	HIO3	
63	I/O		
64	I/O		
65	I/O		
66	GND		
67	I/O	IO8	
68	I/O	IO0	
69	I/O	IO10	
70	I/O	HIO4	
71	VCC	+3.3V	
72	I/O		
73	I/O		
74	I/O	IO9	
75	I/O	IO1	
76	I/O	IO11	
77	INIT -I/O	HIO5	
78	VCC	+3.3V	
79	GND		
80	I/O	IO7	
81	I/O		
82	I/O	IO4	
83	I/O		
84	I/O		
85	I/O		
86	VCC	+3.3V	
87	I/O	IO12	
88	I/O	IO2	
89	I/O	IO14	
90	I/O	HIO6	
91	GND		
92	I/O		
93	I/O		
94	I/O		
95	I/O	IO13	
96	I/O	IO3	
97	I/O	IO15	
98	I/O	HIO7	
99	I/O		
100	I/O		
101	I/O		
102	GCK4 -I/O		
103	GND		
104	DONE	DONE	

208	VCC	+3.3V	
207	GCK8 I/O-		
206	I/O	RW	
205	I/O		
204	I/O	WRITETP	
203	I/O	IOSEL	
202	I/O	IDSEL	
201	I/O	INTSEL	
200	I/O	IPSEL	
199	I/O	A1	
198	I/O		
197	I/O		
196	I/O	A6	
195	GND		
194	I/O	A4	
193	I/O	A5	
192	VCC	+3.3V	
191	I/O		
190	I/O	BS0	
189	I/O	BS1	
188	I/O		
187	I/O		
186	I/O		
185	I/O	TP1	
184	I/O		
183	VCC	+3.3V	
182	GND		
181	I/O		
180	I/O		
179	I/O		
178	I/O	A2	
177	I/O		
176	I/O		
175	I/O		
174	I/O		
173	VCC	+3.3V	
172	I/O	A3	
171	I/O		
170	GND		
169	I/O		
168	I/O		
167	I/O	IO23	
166	I/O	IO22	
165	I/O	IO21	
164	I/O	IO20	
163	I/O	IO19	
162	I/O	IO18	
161	I/O	IO17	
160	I/O	IO16	
159	GCK7 I/O-		
158	GND		
157	TDO (O)-		

156	VCC	+3.3V	
155	CCLK	CCLK	
154	GCK6 I/O-		
153	DIN (DOUT-D0)-	CDATA	
152	I/O	BUFDIR2	
151	I/O	BUF_OE2	
150	I/O		
149	I/O (D1)		
148	I/O		
147	I/O	SPEC_IN	
146	I/O	TP2	
145	I/O	TP3	
144	I/O	IO6	
143	GND		
142	I/O	1DLYDRV	
141	I/O	1DEL20	
140	VCC	+3.3V	
139	I/O	1DEL60	
138	I/O (D2)	1DEL40	
137	I/O	1DEL100	
136	I/O	1DEL80	
135	I/O		
134	I/O	TP4	
133	I/O	IO5	
132	I/O (D3)		
131	GND		
130	VCC	+3.3V	
129	I/O	BUFDIR1	
128	I/O (D4)	BUF_OE1	
127	I/O		
126	I/O	AUX_OUT	
125	I/O	IN2	
124	I/O		
123	I/O	IN1	
122	I/O (D5)		
121	VCC	+3.3V	
120	I/O		
119	I/O	2DLYDRV	
118	GND		
117	I/O	2DEL20	
116	I/O	2DEL60	
115	I/O	2DEL40	
114	I/O	2DEL100	
113	I/O	2DEL80	
112	I/O (D6)		
111	I/O		
110	I/O		
109	I/O (D7)	BUF_OE0	
108	GCK5 I/O-		
107	I/O	BUFDIR0	
106	PROGRAM	RESET	
105	VCC	+3.3V	

C12	100N	+3.3V	
C11	100N		
C10	100N		
C9	100N		
C8	100N		
C5	100N		
C6	100N		
C7	100N	GND	

schematic: XILINX-SYM_REV1

DESY Zeuthen

XILINX FPGA (Rev 1)

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Design	F.TONISCH	7-19-2006_14:00	1 of 1