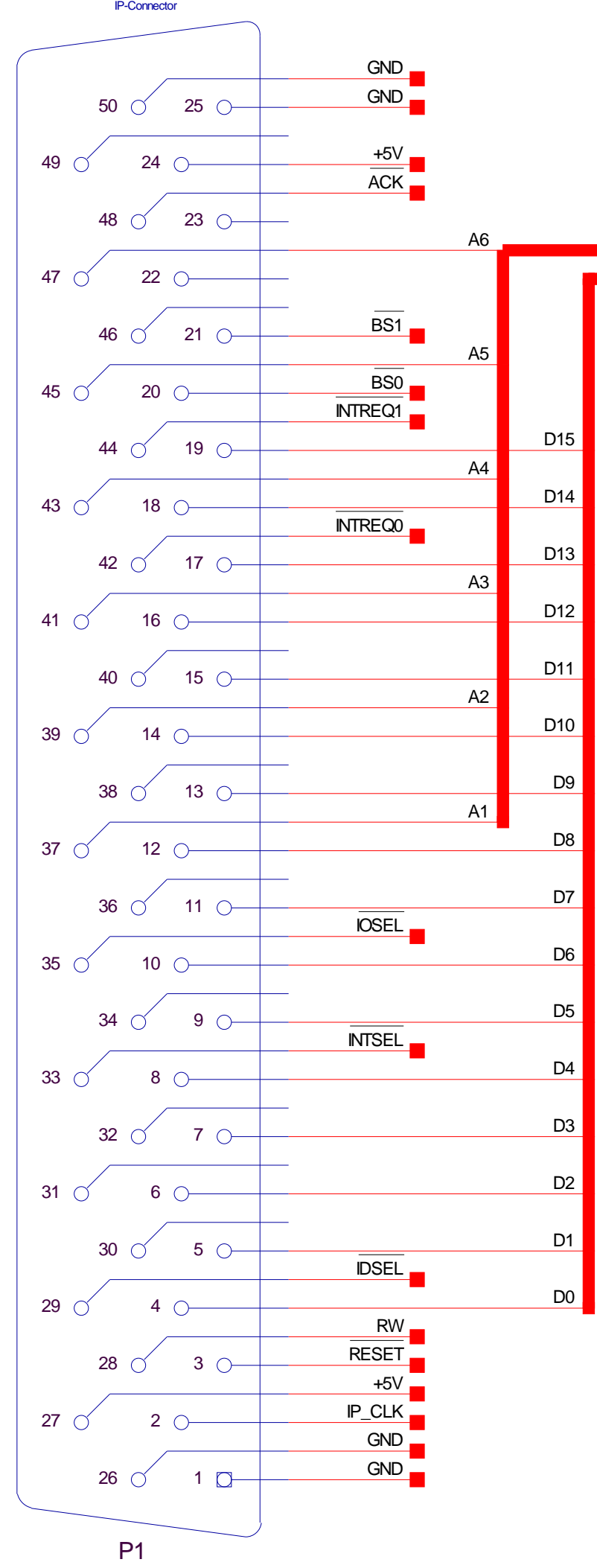
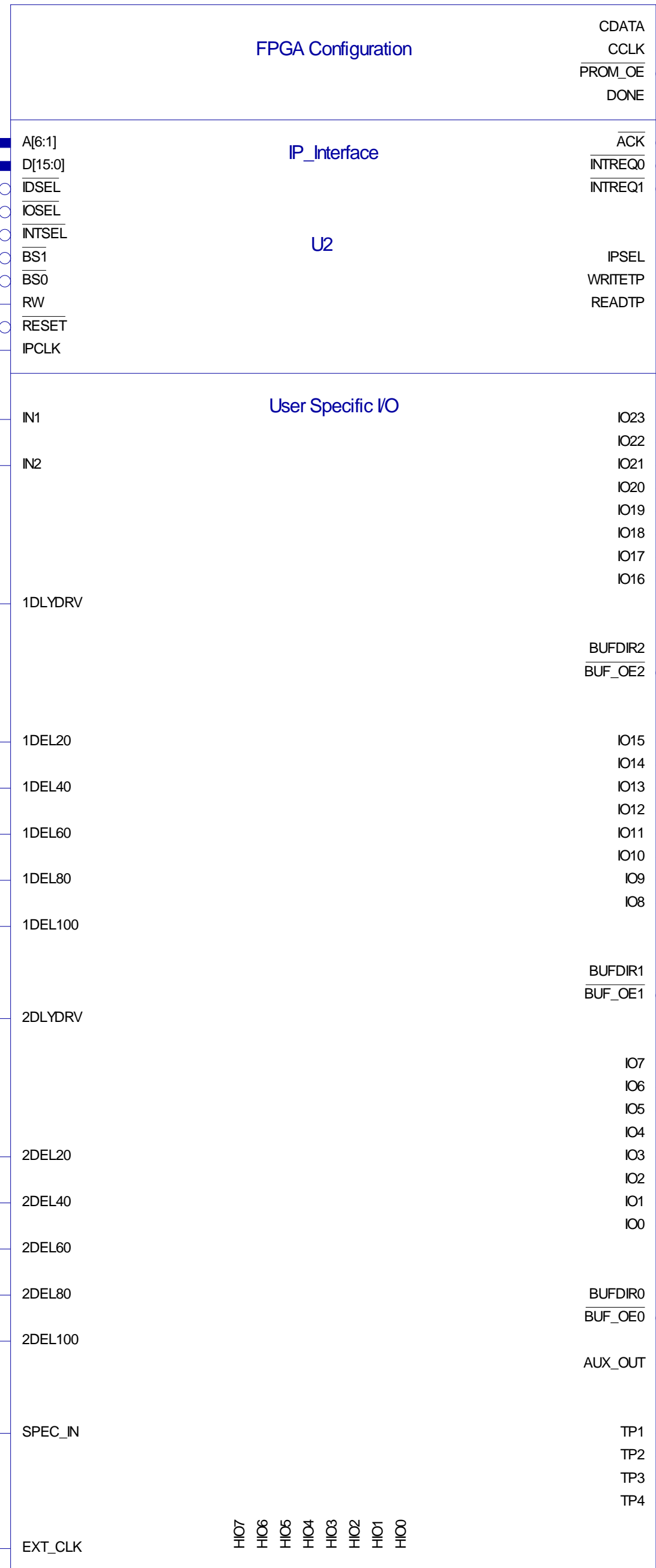


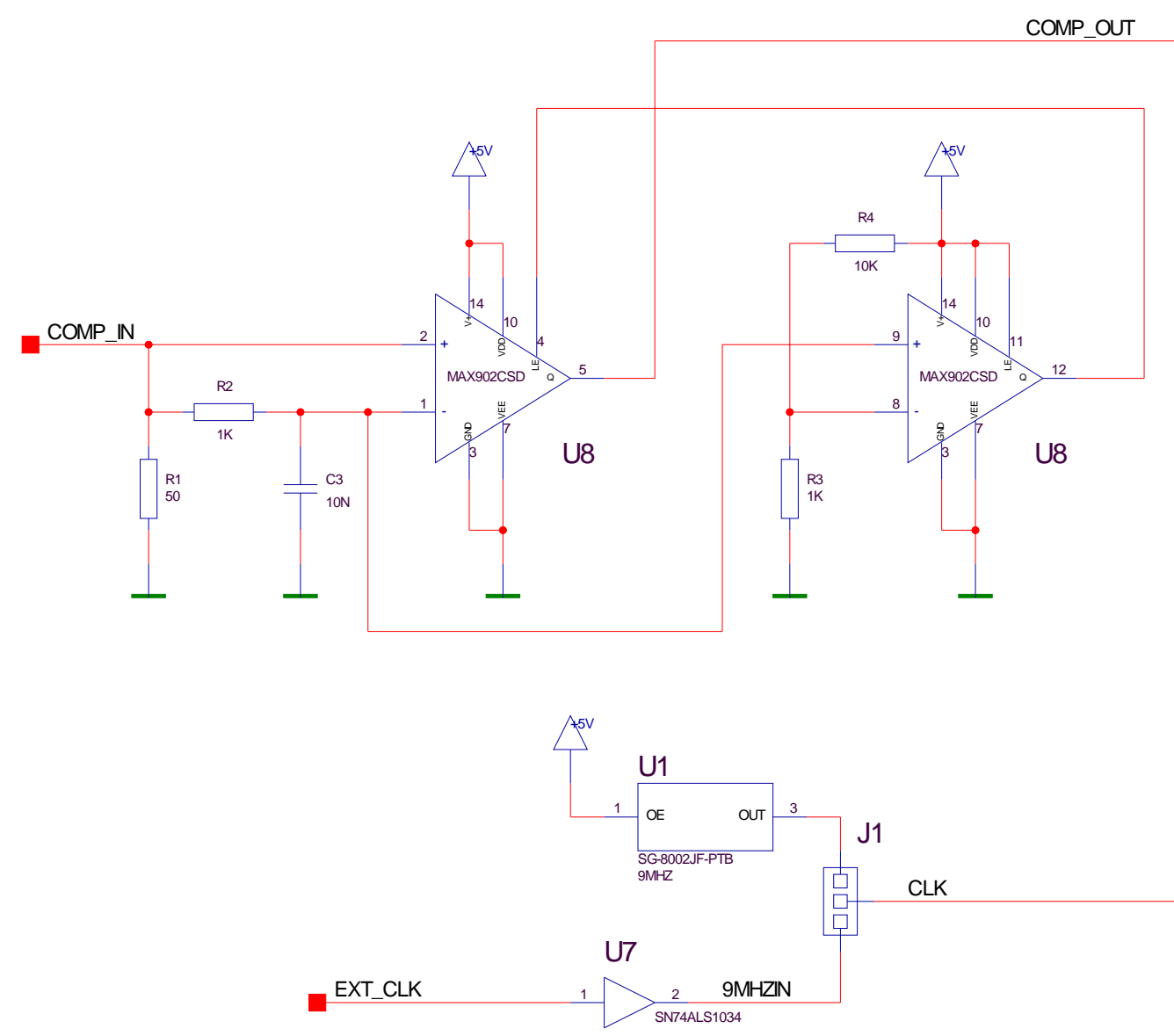
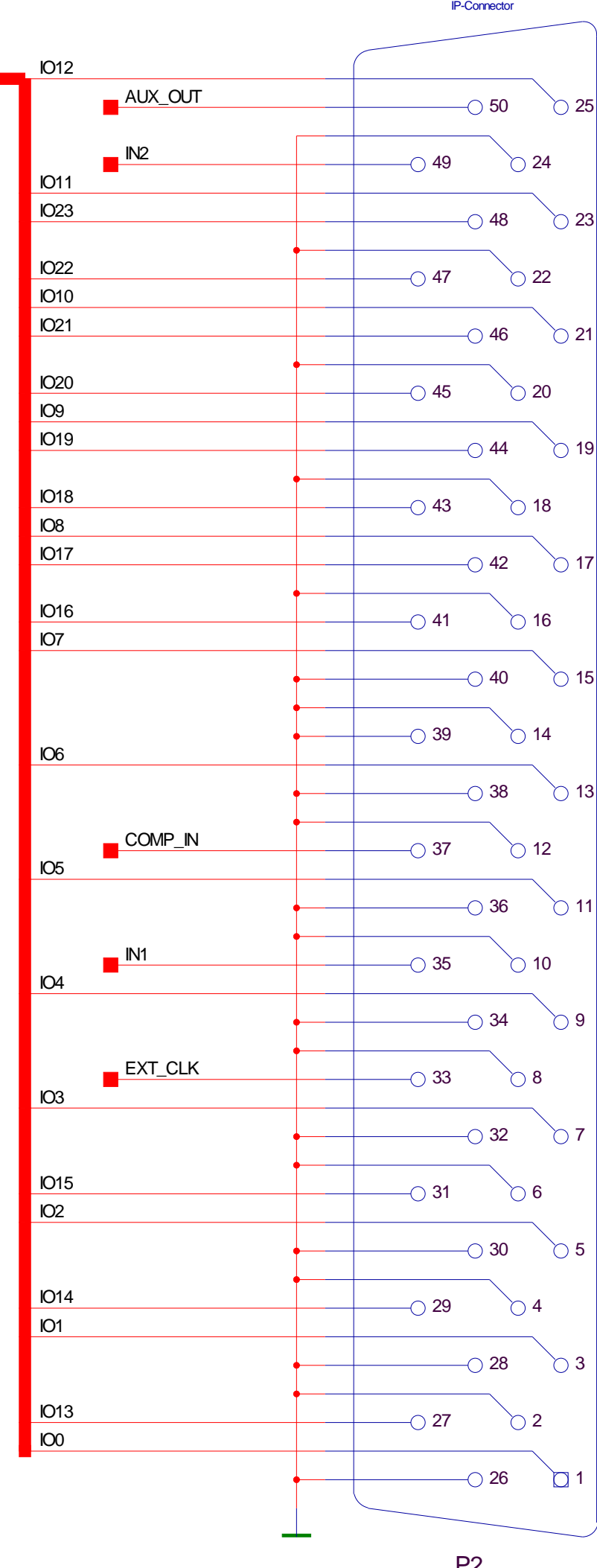
IP Interface Connector



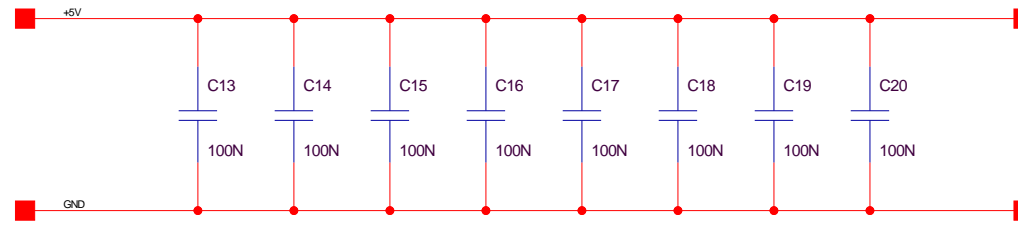
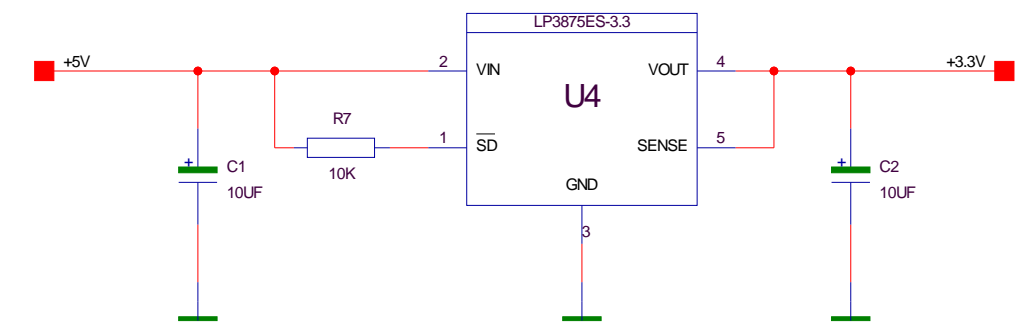
XILINX-SYM



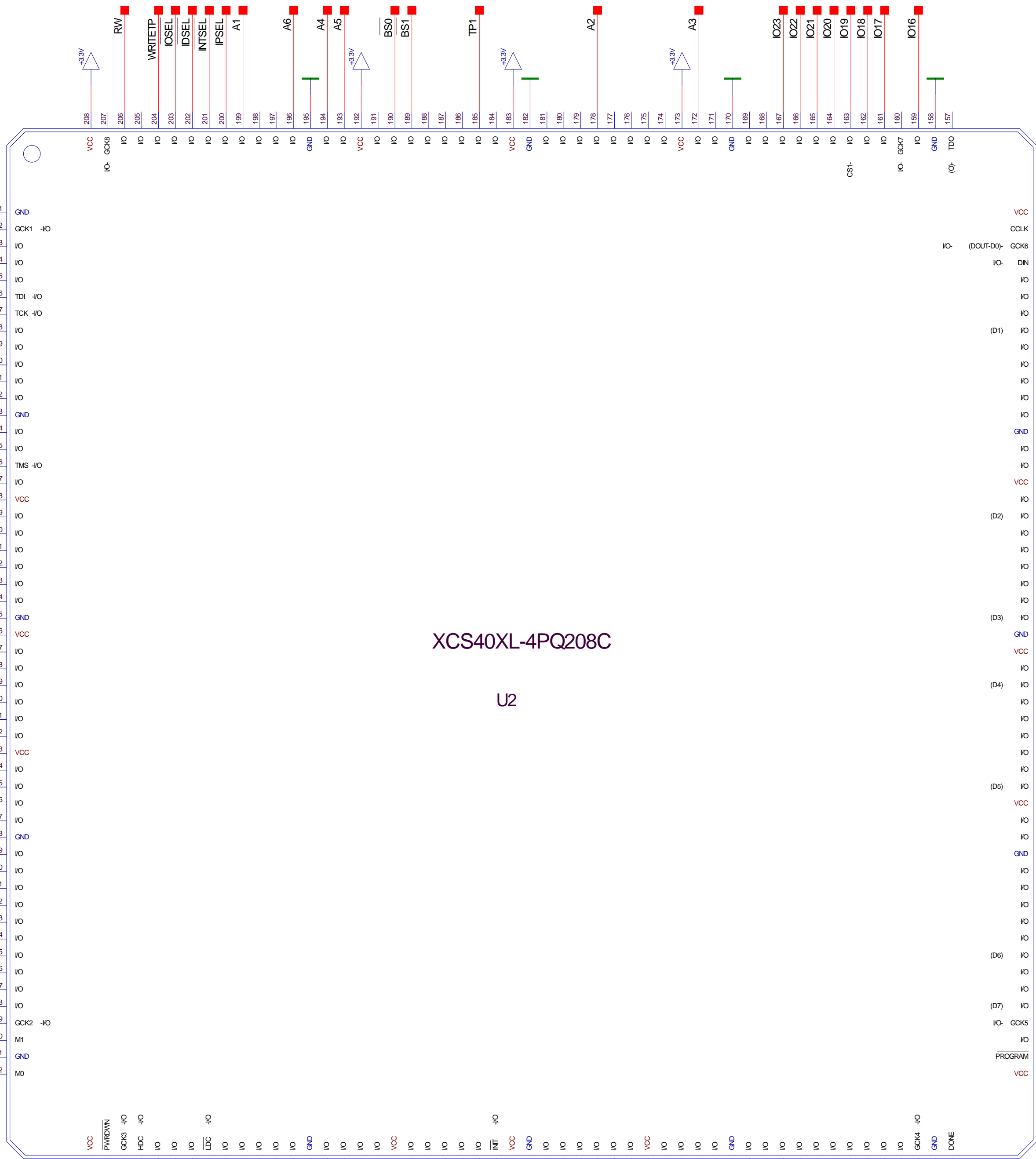
IP - IO - Connector



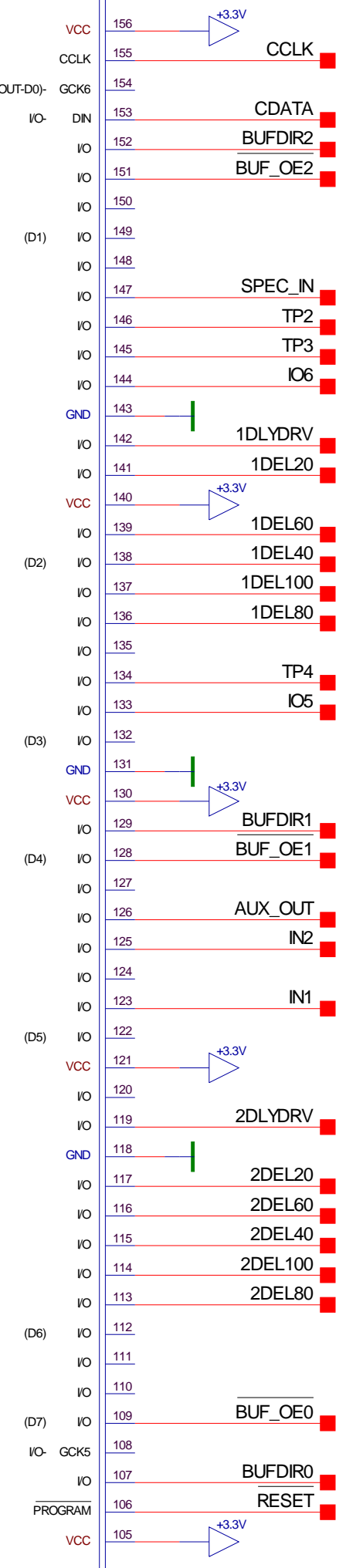
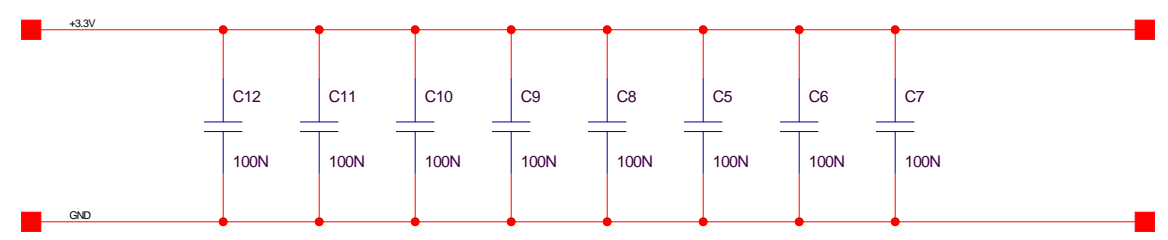
HIO5 is connected to the INIT pin of the XILINX, therefore it cannot be used with jumpers, because then the configuration is not loaded from the PROM! (should be corrected with a new PCB design) Reminder: HIO connection in the actual PCB design is missing, a wire must be soldered.



IP-UNI-XILINX_REV1
Universal I/O Module



XCS40XL-4PQ208C
U2



schematic: XILINX-SYM_REV1



XILINX FPGA (Rev 1)

Drawing	F.TONSCH	Date:	7-19-2006_14:00	Sheet	1 of 1
Design	F.TONSCH				