User manual

IP-UNI-XILINX

Version 1

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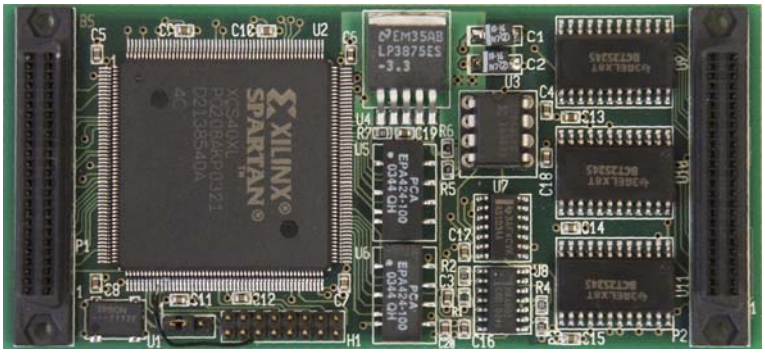

Specifications:

- 24 I/O's with 25Ω Driver capability (in groups of 8 configurable either as input, output or bi-directional I/O)
- 1 comparator input with selftracking threshold
- 2 TTL-compatible logic inputs (50Ω-terminated)
- 1 TTL-compatible clock input for external device clock (50Ω-terminated)
- 1 TTL-compatible output (Iout_low = 24mA)
- XILINX-FPGA XCS40XL containing the IP-Interface and user specified logic, configurable via a serial configuration PROM
- 2 onboard 5-tap delay lines (5 x 20ns)
- 9Mhz crystal oscillator
- 8-bit header for use in decoder functions or to select other user specified options implemented in the FPGA design

1. Description

The IP-UNI-Xilinx is a general purpose digital IndustryPack™ module. It is based on the XCS40XL FPGA of the SpartanXL™-family from XILINX. The use of a FPGA gives to the user full flexibility to implement a design according to the needs. The configuration of the FPGA is loaded from a serial PROM.
On one side the FPGA is directly connected to the IP-Interface connector and on the other side it has connections via buffers to the I/O-connector.
The module provides up to 24 bi-directional I/O lines which are able to drive a load of 25Ω. These lines can be configured in groups of 8 either as input or output or as bidirectional data lines. In addition it has 2 TTL-compatible input lines and one TTL-compatible output line.
An input line to a comparator offers the possibility to connect a signal other then TTL. It must be in the range of 0 to 5V. No threshold setting is necessary because it is selfadjusted to the mean value of the incoming signal.
Two digital 5-tap delay lines driven by the FPGA allow to feedback data.
The FPGA can be clocked either by the internal 9MHz crystal oscillator or by an external clock signal connected via the I/O-connector of the modul. This option is selectable by a jumper.
A 8-bit header is connected to the FPGA. It can be used to monitor some test signals or as a field of jumpers for selectable user options (for instance in decoder applications).

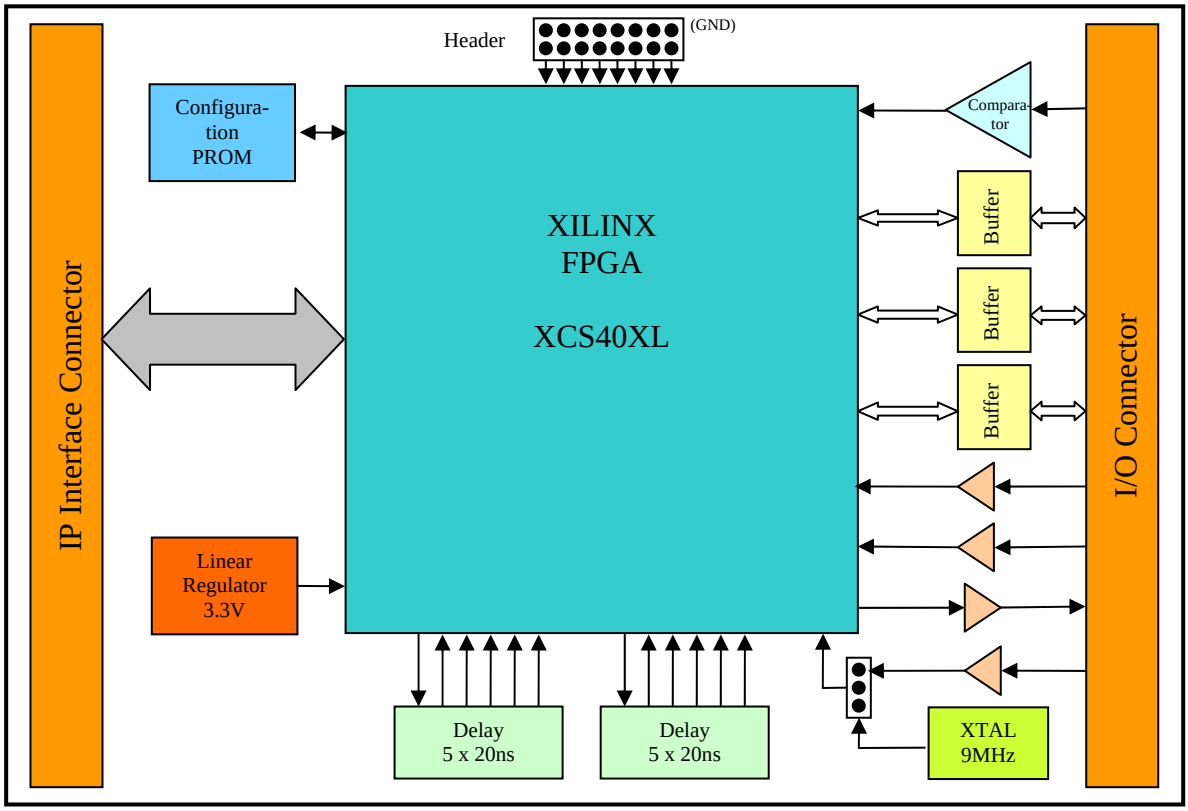

Fig 1: Block scheme

2. FPGA design

The user needs to have a XILINX development environment. The FPGA design can be divided into three major sections:

- the configuration section,
- the IP interface section and
- the user I/O section.

The configuration PROM uses four lines. These lines must not be used in another way.

In the second section all connections to the IP interface are defined. There are 16 bi-directional data lines, 6 address lines and 8 control lines and 2 interrupt lines. In addition 3 test points at the solder side of the module are connected to the XILINX FPGA. The following IP cycles can be implemented:

- IO cycle (IOSEL)
- ID cycle (IDSEL), where the ID-PROM will be implemented in the FPGA itself
- Interrupt cycle (INTSEL).

Neither DMA nor memory cycles can be implemented because of the lack of connections to the interface connector. The reset line provokes a re-load of the XILINX configuration and sets all internal flip flops to an initial state.
Schematics of a reference design for the IP interface logic can be delivered. The schematics were drawn with the DxDesigner from Mentor Graphics. In the future some VHDL input may be available.

In the third section the I/O pins of the module are definded. The usage of these connections depends on the user design. Two delay lines offer the possibility to feed back logic signals with pre-defined delay to the FPGA.

A complete listing of pin numbers and types of the FPGA is given in appendix C. The location of these pins should be fixed in a user constraint file (UCF) to avoid damage of the FPGA.

Pins not used in the design are automatically set to tri-state by the XILINX software.

A. IP Interface connections (P1)

Signal	Pin #		Signal
GND	**1**	**2**	CLK
RESET~	**3**	**4**	D0
D1	**5**	**6**	D2
D3	**7**	**8**	D4
D5	**9**	**10**	D6
D7	**11**	**12**	D8
D9	**13**	**14**	D10
D11	**15**	**16**	D12
D13	**17**	**18**	D14
D15	**19**	**20**	BS0*
BS1*	**21**	**22**	
	23	**24**	+5V
GND	**25**	**26**	GND
+5V	**27**	**28**	RW
IDSEL*	**29**	**30**	
	31	**32**	
INTSEL*	**33**	**34**	
IOSEL*	**35**	**36**	
A1	**37**	**38**	
A2	**39**	**40**	
A3	**41**	**42**	INTREQ0
A4	**43**	**44**	INTREQ1
A5	**45**	**46**	
A6	**47**	**48**	ACK
	49	**50**	GND

Table 1: IP-Interface

B. I/O connections (P2)

Signal	Pin #		Signal
IO0	**1**	**2**	GND
IO1	**3**	**4**	GND
IO2	**5**	**6**	GND
IO3	**7**	**8**	GND
IO4	**9**	**10**	GND
IO5	**11**	**12**	GND
IO6	**13**	**14**	GND
IO7	**15**	**16**	GND
IO8	**17**	**18**	GND
IO9	**19**	**20**	GND
IO10	**21**	**22**	GND
IO11	**23**	**24**	GND
IO12	**25**	**26**	GND
IO13	**27**	**28**	GND
IO14	**29**	**30**	GND
IO15	**31**	**32**	GND
EXT_CLK	**33**	**34**	GND
IN1	**35**	**36**	GND
COMP_IN	**37**	**38**	GND
GND	**39**	**40**	GND
IO16	**41**	**42**	IO17
IO18	**43**	**44**	IO19
IO20	**45**	**46**	IO21
IO22	**47**	**48**	IO23
IN2	**49**	**50**	AUX_OUT

Table 2: I/OConnector

C. XILINX connections

	Logic Block		IP-UNI-XILINX		
			Name	Type	Pin #
1	IP-Interface & Configuration	Confiuration PROM	CDATA	INPUT	P153
2			CCLK	INPUT	P155
3			LDS	OUTPUT	P60
4			DONE	OUTPUT	P104
5		Control Lines	IDSEL	INPUT	P202
6			IOSEL	INPUT	P203
7			INTSEL	INPUT	P201
8			ACK	OUTPUT	P5
9			BS0	INPUT	P190
10			BS1	INPUT	P189
11			RW	INPUT	P206
12			RESET	INPUT	P106
13		Interrupt Lines	INTREQ0	OUTPUT	P27
14			INTREQ1	OUTPUT	P20
15		Address Lines	A1	INPUT	P199
16			A2	INPUT	P178
17			A3	INPUT	P172
18			A4	INPUT	P194
19			A5	INPUT	P193
20			A6	INPUT	P196
21		Data Lines	D0	BIDIR	P36
22			D1	BIDIR	P37
23			D2	BIDIR	P34
24			D3	BIDIR	P35
25			D4	BIDIR	P31
26			D5	BIDIR	P32
27			D6	BIDIR	P30
28			D7	BIDIR	P29
29			D8	BIDIR	P23
30			D9	BIDIR	P24
31			D10	BIDIR	P17
32			D11	BIDIR	P16
33			D12	BIDIR	P8
34			D13	BIDIR	P9
35			D14	BIDIR	P15
36			D15	BIDIR	P14
37		Test Point	IPSEL (TP1)	OUTPUT	P200
38			READTP (TP3)	OUTPUT	P3
39			WRITETP (TP2)	OUTPUT	P204
40		Clock	IPCLK	INPUT	P49

Table 3: FPGA Pinout

	Logic Block		IP-UNI-XILINX		
			Name	Type	Pin #
41	User I/O	IO-Buffer0	BUFFDIR0	OUTPUT	P107
42			BUFF_OE0	OUTPUT	P109
43			IO0	BIDIR	P68
44			IO1	BIDIR	P75
45			IO2	BIDIR	P88
46			IO3	BIDIR	P96
47			IO4	BIDIR	P82
48			IO5	BIDIR	P133
49			IO6	BIDIR	P144
50			IO7	BIDIR	P80
51		IO-Buffer1	BUFFDIR1	OUTPUT	P129
52			BUFF_OE1	OUTPUT	P128
53			IO8	BIDIR	P67
54			IO9	BIDIR	P74
55			IO10	BIDIR	P69
56			IO11	BIDIR	P76
57			IO12	BIDIR	P87
58			IO13	BIDIR	P95
59			IO14	BIDIR	P89
60			IO15	BIDIR	P97
61		IO-Buffer2	BUFFDIR2	OUTPUT	P152
62			BUFF_OE2	OUTPUT	P151
63			IO16	BIDIR	P159
64			IO17	BIDIR	P161
65			IO18	BIDIR	P162
66			IO19	BIDIR	P163
67			IO20	BIDIR	P164
68			IO21	BIDIR	P165
69			IO22	BIDIR	P166
70			IO23	BIDIR	P167

Table 4: FPGA Pinout (cont.)

	Logic Block		IP-UNI-XILINX		
			Name	Type	Pin #
71	User I/O	Inputs	SPEC_IN	INPUT	P147
72			IN1	INPUT	P123
73			IN2	INPUT	P125
74		Output	AUX_OUT	OUTPUT	P126
75		Delay1	1DLYDRV	OUTPUT	P142
76			1DEL20	INPUT	P141
77			1DEL40	INPUT	P138
78			1DEL60	INPUT	P139
79			1DEL80	INPUT	P136
80			1DEL100	INPUT	P137
81		Delay2	2DLYDRV	OUTPUT	P119
82			2DEL20	INPUT	P117
83			2DEL40	INPUT	P115
84			2DEL60	INPUT	P116
85			2DEL80	INPUT	P113
86			2DEL100	INPUT	P114
87		Test Points	TP5	OUTPUT	P185
88			TP6	OUTPUT	P146
89			TP7	OUTPUT	P145
90			TP8	OUTPUT	P134
91		Header	HIO0	BIDIR	P58
92			HIO1	BIDIR	P59
93			HIO2	BIDIR	P61
94			HIO3	BIDIR	P62
95			HIO4	BIDIR	P70
96			HIO5	BIDIR	P77
97			HIO6	BIDIR	P90
98			HIO7	BIDIR	P98
99		Clock	Ext_CLK	INPUT	P2

Table 5: FPGA Pinout (cont.)