User Manual

Clock Generator Unit

Rev. 1.0

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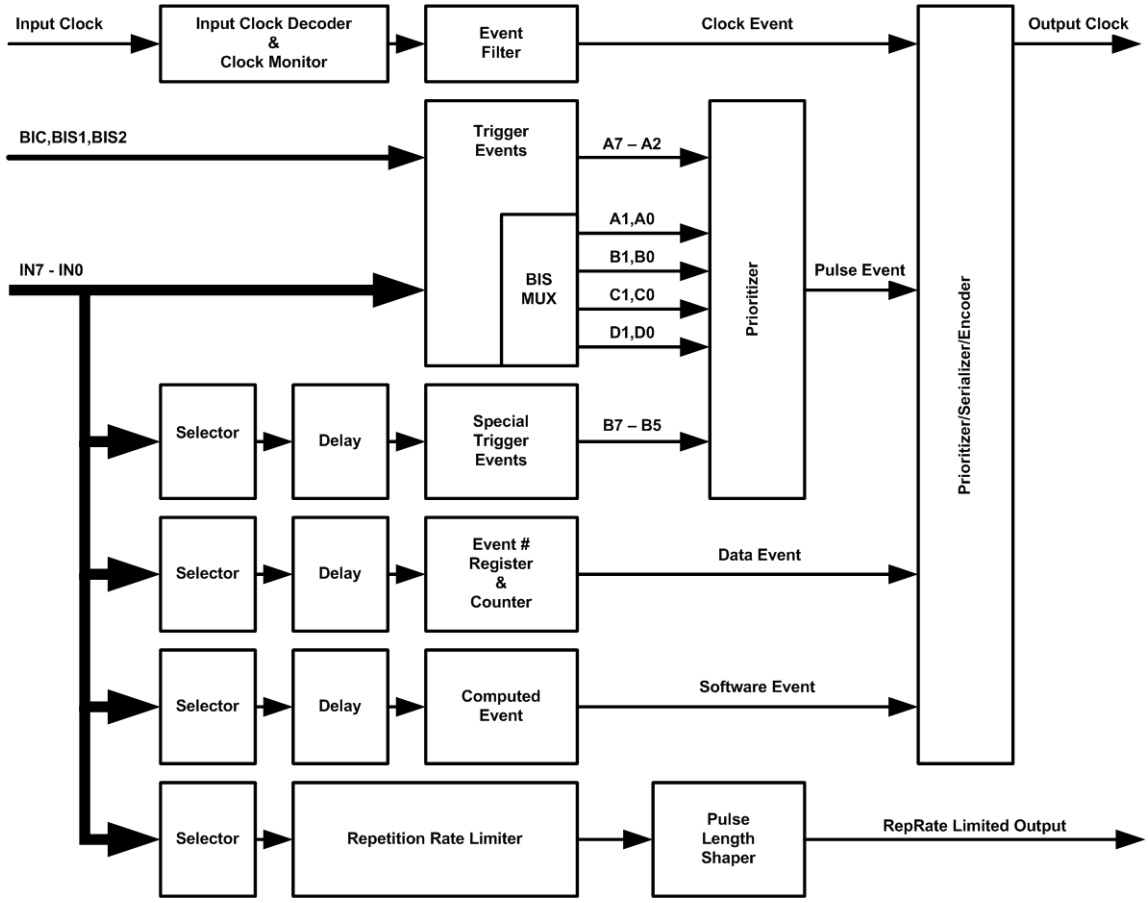
Specifications:

- IP Interface Logic
- Manchester Encoder for events from 8 trigger inputs
- Manchester Decoder for incoming clock events
- 32-bit Event Number Counter
- Computed Event Generator
- Repetition Rate Limiter

1 Introduction

The design of the Clock Generator is based on the IP-UNI-XILINX board, a general purpose digital I/O module containing a XILINX XCS40XL FPGA.

Figure 1: Simplified Block Diagram



It creates 8-bit event messages on a serial output clock line with a start bit preceding and a parity bit following. A kind of Manchester Encoding is used. A logic *1* is represented by a transition in the middle of the bit whereas no transmission indicates a logic *0* (see Figure 2). These messages are received and decoded by Delay Timer Units for the synchronization of devices along the FLASH facility.

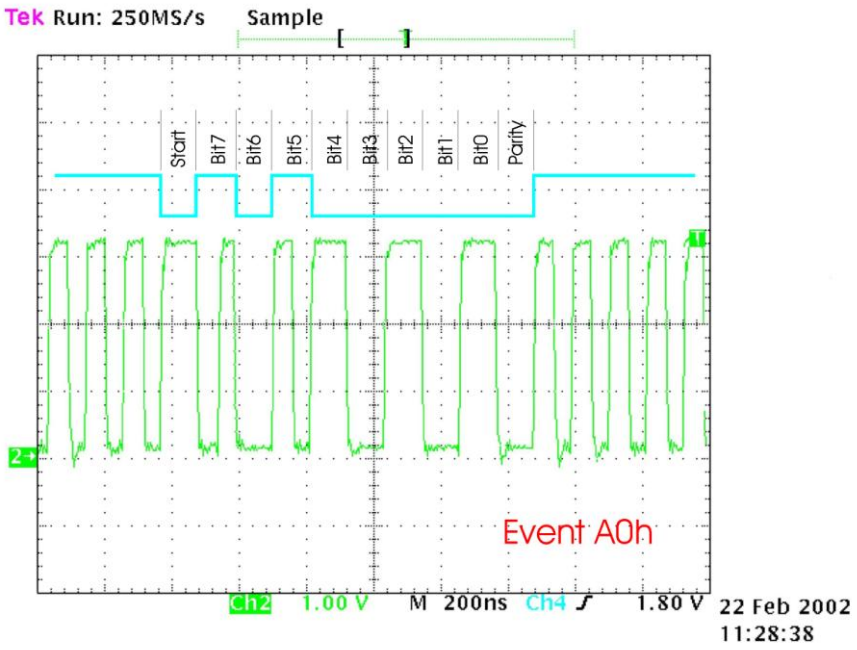
There are two general types of event sources: Triggered by external signals or generated by the computer itself.

From external the unit either detects an event message on the incoming clock or one or more of 8 input lines received a trigger.

A 32-bit data word may be send as a set of ten events or a computed event will be generated by writing to a single register. Recently only a32-bit event number is send to the Delay Timers. In later

versions more data types could be send to transmit generalized status information to other devices. The transmission may be synchronized by external signals from the inputs IN7-IN0.

Figure 2: Example of a Clock Output Signal



Signals from the beam inhibit system (BIC, BIS1, BIS2) are used to generate special events defining the running mode of the accelerator.

A special output signal with repetition rate limitation is generated. It may be used to protect the system and prevent damages due to too high trigger rate at the pulsed inputs. Which trigger signal is used for repetition rate limitation can be set in register at location *0x0F* as well as the maximum allowed output cycle time. The default event value is *0xA6* and the cycle time is set to 64ms (~15.6Hz).

2 Event Description

2.1 Pulsed Events

Pulse inputs are latched, prioritized and output as events *0xWn* where *W* is a 4-bit value set by D3-D0 in the register located at *base + 0x00* (default value is *0xA*). The value *n* of the lower four bits depends on which input line was pulsed and on the value of bit D4 in register at *base + 0x02*. For D4=0 the value *n* ranges from *0x0* to *0x7* and for D4=1 the range of *n* is *0x8* to *0xF*. The bigger the value is the higher is the priority of the event. Event with the highest priority is send first.

There are some special events generated: *0xX7*, *0xX6*, *0xX5* where *X* is a 4-bit value set by D7-D4 in the register located at *base + 0x00* (default value is *0xB*). One has to select 1 of the 8 inputs to trigger these events in the register at *base + 0x08* (D2-D0). The trigger can be enabled/disabled writing a 1/0 to D4 in that register. The event output can be delayed by writing to D14-D8 (default is 0). The delay time depends on which time base has been chosen. The bits D7 and D6 define the time base for the delay counter (default is 1ms). D15 enables or disables the output from the delay counter (default is 1). The output from the delay counter is fed to a threefold delay counter with fixed delay of 3, 6 or 9µs. These three outputs are then fed to dividers by 64, 32 and 16 thus generating the events *0xX7*, *0xX6* and *0xX5* every n^{th} cycle accordingly.

Table 1: Time base for Delay Counter (reg. at *base+0x08*)

D7	D6	Time Base
0	0	110ns
0	1	1µs
1	0	1ms

Depending on the inputs BIC, BIS1 and BIS2 from the beam inhibit system a second kind of specialized pulsed events are generated: *0xYn* where *Y* is a 4-bit value set by D11-D8 in the register located at *base + 0x00* (default value is *0xC*) and *0xZn* where *Z* is a 4-bit value set by D15-D12 in the register located at *base + 0x00* (default value is *0xD*). The value of n depends on which input the pulsed event was received (see Table 2 and Table 3).

Table 2: Triggered from In1

BIS2	BIS1	Output
0	0	*0xW1*
0	1	*0xX1*
1	0	*0xY1*
1	1	*0xZ1*

Table 3: Triggered from In0

BIC	BIS2	BIS1	Output
0	0	0	*0xW0*
x	0	1	*0xX0*
x	1	0	*0xY0*
1	x	0	
0	1	1	*0xZ0*

Pulsed events have the highest priority prior other events described later on.

2.2 Input Clock Events

If there are more than one Clock Generator in the system the events decoded from incoming clock with values in the same range of pulsed events can be either blocked or passed. For blocking the appropriate bits D3-D0 in register *base + 0x02* must be set to one.

2.3 Event Number Transmission

A special set of event values have been reserved for transmission of 32-bit data over the clock line. It ranges from *0x0n* to *0x2n*.

Event Value:	Function:	where:
0x1m	Start Transmission	*m* = Address in Destination RAM
$0x0y_0$ - $0x0y_7$	8 x 4bit Data	y_n = Data Nibble 0-7
0x2m	End of Transmission	*m* = Address in Destination RAM (for validation)

A data transmission is initiated by sending *0x1m*, where the value *m* is interpreted in the receiver module (Delay Timer) into which location of 32-bit wide RAM the data will be written. The 32-bit data are transmitted in portions of eight 4-bit nibbles and send as $0x0y_0$ - $0x0y_7$ events. The data then are validated by sending *0x2m*. A logic in the receiver unit (e.g. in conjunction with a timeout counter) could then check if the transmission was complete and in case it was incomplete set an error flag.

In the current design of the Clock Generator only *x=0* is implemented which means event number data will follow. More data types can be defined and implemented in later versions of the design.

A 32-bit counter is incremented by a pulsed event selected by D2-D0 of the register at *base + 0x0A*. It starts a 7-bit delay counter. The delayed output from the delay counter initiates the data transmission if D4 and D15 in register at *base + 0x0A* is set to *1*. Time base and output delay is set in a similar way as for special pulsed events (compare 2.1 *Pulsed Events* page 5). The counter can be preset by write data to locations *base + 0x04* (low word) and *base +0x06* (high word). Reading from this location gives the actual event count.

2.4 Computed Events

Computer generated events are another type of events. Writing to register location *base + 0x0E* will cause the value written to be encoded on the serial clock. The event encoding starts either asynchronously if the output of the delay counter is disabled (D15=0 in register at *base + 0x0C*) or is synchronized with a pulsed event selected by D2-D0 in the register at location *base + 0xC* and delayed depending on the contents of the delay settings and the chosen time base.

Computed events have the lowest priority.

3 I/O Address Mapping

Address Offset	Mode	Bit # 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	default value
0x00	W	D-Event				C-Event				B-Event				A-Event				0xDCBA
	R																	
0x02	W								9MHz Clock Status				EVENT Range	Enable D-Mask	Enable C-Mask	Enable B-Mask	Enable A-Mask	0x0100*
	R																	
0x04	W	Initial Event Number (low word)																0x0000
	R	Actual Event Number read back (low word)																
0x06	W	Initial Event Number (high word)																0x0000
	R	Actual Event Number read back (high word)																
0x08	W	Enable Output	Output Delay for B-Event Request							Time Base for delay counter			B-Event Enable		B7-B5 Trigger Event Selection			0x8096
	R																	
0x0A	W	Enable Output	Output Delay for Event Number Request							Time Base for delay counter			Event # Enable		Trigger Event for Event Number Increment			0x8096
	R																	
0x0C	W	Enable Output	Output Delay for Computed Event Request							Time Base for delay counter			C-Event Enable		Sync Event for Computed Event			0x8096
	R																	
0x0E	W									Computed Event								0x0000
	R																	
0x10	W	Repetition Rate Limit [ms]												Pulse Length	Rep-rate Limited Event			0x800F
	R																	

Table 4: Register Mapping

A. IP Interface connections (P1)

Pin #	Timer	Pin #	Timer
1	GND	2	CLK
3	RESET~	4	D0
5	D1	6	D2
7	D3	8	D4
9	D5	10	D6
11	D7	12	D8
13	D9	14	D10
15	D11	16	D12
17	D13	18	D14
19	D15	20	
21		22	
23		24	+5V
25	GND	26	GND
27	+5V	28	RW
29	IDSEL*	30	
31		32	
33	INTSEL*	34	
35	IOSEL*	36	
37	A1	38	
39	A2	40	
41	A3	42	INTREQ0
43	A4	44	
45	A5	46	
47	A6	48	ACK
49		50	GND

B. I/O connections (P2)

Pin #	Timer	Pin #	Timer
1	CLOCK_OUT_0	2	GND
3	CLOCK_OUT_1	4	GND
5	CLOCK_OUT_2	6	GND
7	CLOCK_OUT_3	8	GND
9	10Hz_OUT	10	GND
11	9MHz_OUT	12	GND
13	*reserve*	14	GND
15	*reserve*	16	GND
17	EVENT_0	18	GND
19	EVENT_1	20	GND
21	EVENT_2	22	GND
23	EVENT_3	24	GND
25	EVENT_4	26	GND
27	EVENT_5	28	GND
29	EVENT_6	30	GND
31	EVENT_7	32	GND
33	EXT_9MHZ	34	GND
35	BIC	36	GND
37	EVENTCLK_IN	38	GND
39	GND	40	GND
41	BIS1	42	BIS2
43	*reserve*	44	*reserve*
45	*reserve*	46	*reserve*
47	*reserve*	48	*reserve*
49	*reserve*	50	*reserve*

C. XILINX Pinout

	Logic Block		IP-UNI-XILINX			VUVFEL ClockGen	
			Name	Type	Pin #	Name	Type
1	IP-Interface & Configuration	Configuration PROM	CDATA	INPUT	P153	CDATA	INPUT
2			CCLK	INPUT	P155	CCLK	INPUT
3			LDS	OUTPUT	P60	PROM_OE	OUTPUT
4			DONE	OUTPUT	P104	DONE	OUTPUT
5		Control Lines	IDSEL	INPUT	P202	IDSEL-	INPUT
6			IOSEL	INPUT	P203	IOSEL-	INPUT
7			INTSEL	INPUT	P201	INTSEL-	INPUT
8			ACK	OUTPUT	P5	ACK-	OUTPUT
9			BS0	INPUT	P190	BS0-	INPUT
10			BS1	INPUT	P189	BS1-	INPUT
11			RW	INPUT	P206	RW	INPUT
12			RESET	INPUT	P106	RESET	INPIT
13		Interrupt Lines	INTREQ0	OUTPUT	P27		
14			INTREQ1	OUTPUT	P20		
15		Address Lines	A1	INPUT	P199	IPA1	INPUT
16			A2	INPUT	P178	IPA2	INPUT
17			A3	INPUT	P172	IPA3	INPUT
18			A4	INPUT	P194	IPA4	INPUT
19			A5	INPUT	P193	IPA5	INPUT
20			A6	INPUT	P196	IPA6	INPUT
21		Data Lines	D0	BIDIR	P36	IPDATA0	BIDIR
22			D1	BIDIR	P37	IPDATA1	BIDIR
23			D2	BIDIR	P34	IPDATA2	BIDIR
24			D3	BIDIR	P35	IPDATA3	BIDIR
25			D4	BIDIR	P31	IPDATA4	BIDIR
26			D5	BIDIR	P32	IPDATA5	BIDIR
27			D6	BIDIR	P30	IPDATA6	BIDIR
28			D7	BIDIR	P29	IPDATA7	BIDIR
29			D8	BIDIR	P23	IPDATA8	BIDIR
30			D9	BIDIR	P24	IPDATA9	BIDIR
31			D10	BIDIR	P17	IPDATA10	BIDIR
32			D11	BIDIR	P16	IPDATA11	BIDIR
33			D12	BIDIR	P8	IPDATA12	BIDIR
34			D13	BIDIR	P9	IPDATA13	BIDIR
35			D14	BIDIR	P15	IPDATA14	BIDIR
36			D15	BIDIR	P14	IPDATA15	BIDIR
37		Test Point	IPSEL	OUTPUT	P200	IPSEL	OUTPUT
38			READTP	OUTPUT	P3	READTP	OUTPUT
39			WRITETP	OUTPUT	P204	WRITETP	OUTPUT
40		Clock	IPCLK	INPUT	P49	8MHZIN	INPUT

	Logic Block		IP-UNI-XILINX			VUVFEL ClockGen	
			Name	Type	Pin #	Name	Type
41	User Space	IO-Buffer0	BUFFDIR0	OUTPUT	P107	Logic 0	INPUT
42			BUFF_OE0	OUTPUT	P109	Logic 0	INPUT
43			IO0	BIDIR	P68	CLOCK_OUT0	OUTPUT
44			IO1	BIDIR	P75	CLOCK_OUT1	OUTPUT
45			IO2	BIDIR	P88	CLOCK_OUT2	OUTPUT
46			IO3	BIDIR	P96	CLOCK_OUT3	OUTPUT
47			IO4	BIDIR	P82	LIM_OUT	OUTPUT
48			IO5	BIDIR	P133		
49			IO6	BIDIR	P144		
50			IO7	BIDIR	P80		
51		IO-Buffer1	BUFFDIR1	OUTPUT	P129	Logic 1	INPUT
52			BUFF_OE1	OUTPUT	P128	Logic 0	INPUT
53			IO8	BIDIR	P67	In0	INPUT
54			IO9	BIDIR	P74	In1	INPUT
55			IO10	BIDIR	P69	In2	INPUT
56			IO11	BIDIR	P76	In3	INPUT
57			IO12	BIDIR	P87	In4	INPUT
58			IO13	BIDIR	P95	In5	INPUT
59			IO14	BIDIR	P89	In6	INPUT
60			IO15	BIDIR	P97	In7	INPUT
61		IO-Buffer2	BUFFDIR2	OUTPUT	P152	Logic 1	INPUT
62			BUFF_OE2	OUTPUT	P151	Logic 0	INPUT
63			IO16	BIDIR	P159	BIS1	INPUT
64			IO17	BIDIR	P161	BIS2	INPUT
65			IO18	BIDIR	P162		
66			IO19	BIDIR	P163		
67			IO20	BIDIR	P164		
68			IO21	BIDIR	P165		
69			IO22	BIDIR	P166		
70			IO23	BIDIR	P167		

	Logic Block		IP-UNI-XILINX			VUVFEL ClockGen	
			Name	Type	Pin #	Name	Type
71	User Space	Inputs	SPEC_IN	INPUT	P147	TCLKIN	INPUT
72			IN1	INPUT	P123	BIC	INPUT
73			IN2	INPUT	P125		
74		Output	AUX_OUT	OUTPUT	P126	INDICATOR	OUTPUT
75		Delay1	1DLYDRV	OUTPUT	P142	1DLYDRV	OUTPUT
76			1DEL20	INPUT	P141	1DEL20	INPUT
77			1DEL40	INPUT	P138	1DEL40	INPUT
78			1DEL60	INPUT	P139	1DEL60	INPUT
79			1DEL80	INPUT	P136	1DEL80	INPUT
80			1DEL100	INPUT	P137	1DEL100	INPUT
81		Delay2	2DLYDRV	OUTPUT	P119	2DLYDRV	OUTPUT
82			2DEL20	INPUT	P117	2DEL20	INPUT
83			2DEL40	INPUT	P115	2DEL40	INPUT
84			2DEL60	INPUT	P116	2DEL60	INPUT
85			2DEL80	INPUT	P113	2DEL80	INPUT
86			2DEL100	INPUT	P114	2DEL100	INPUT
87		Test Point	TP1	OUTPUT	P185	SDATA_OUT	OUTPUT
88			TP2	OUTPUT	P146	BUSY_OUT	OUTPUT
89			TP3	OUTPUT	P145	DONE_OUT	OUTPUT
90			TP4	OUTPUT	P134	CDATA_OUT	OUTPUT
91		Header	HIO0	BIDIR	P58	P_REQ_OUT	OUTPUT
92			HIO1	BIDIR	P59	CLK_REQ_OUT	OUTPUT
93			HIO2	BIDIR	P61	EV_NR_REQ_OUT	OUTPUT
94			HIO3	BIDIR	P62	COMP_REQ_OUT	OUTPUT
95			HIO4	BIDIR	P70	9MHZ_CLOCK_OUT	OUTPUT
96			HIO5	BIDIR	P77	SEND_REQ	OUTPUT
97			HIO6	BIDIR	P90	SEND	OUTPUT
98			HIO7	BIDIR	P98	STOP	OUTPUT
99		Clock	Ext_CLK	INPUT	P2	9MHZ_CLK_IN	INPUT