V1495_TLU Interface
-
a programmed implementation for the CAEN V1495 module

by H. Henschel
- DESY -

August 2013, updated in January 2014

1. Overview

The **V1495 TLU Interface** acts as an experiment bound counterpart for the DESY test-beam trigger controller **TLU**. It responds to the 'Trigger Data Handshake' as described in the TLU documentation, chapter 5.1 (and, as well, to the 'Simple Handshake').

A VME register interface allows the experiment DAQ to control the handshake.

In 'Trigger Data Handshake' mode the module receives the TLU TRIGGER, asserts the corresponding BUSY and the 15 required clock pulses (T_CLK). While sending the clock it receives the Trigger DATA as sent by the TLU. In 'Simple Handshake' mode the module receives the TLU TRIGGER and asserts the corresponding BUSY. In both modes the handshake is reset when the experiment DAQ signals that the readout has finished.

The interface is programmed into a CAEN V1495 module with a NIM I/O mezzanine plugged to port 'F'. All January 2014 updates are backward compatible with December 2013 version (firmware 9.9), except for the Test mode.

2. Function

The TRIGGER ist instantly recognized in the V1495_TLU and latched asynchronously. The V1495_TLU will assert BUSY automatically upon latching a trigger.
In 'Trigger Data Handshake' mode the V1495_TLU will generate a sequence of 16 clock pulses (~5MHz) sent on the T_CLK line. Following each clock the V1495_TLU will latch the signal level on the TRIGGER line and store it in a shift register (least significant bit first in).
While the clock sequence is sent the module keeps the 'BUSY' signal asserted. It is cleared after the last clock pulse.
The user may check for the end of this clock sequence by reading bit 1 of the *Trigger Register* ('READY'); thereafter the trigger number may be read from the *Pattern Register*.
By reading this register the module is cleared for a new trigger (short pulse of the 'DONE' signal).

The V1495_TLU may be programmed to operate the T_CLK line as a VETO for further triggers by setting it to logic '1' while the module waits for the trigger number to be read. This is done by setting bit 1 of the *Status Register* to '1'.

The V1495_TLU provides a 'clean' trigger output for other DAQ modules: a single 25ns pulse (with any succeeding Trigger DATA transmission supressed). This 'clean' trigger is however synchronized to the module's internal clock, hence shows a jitter of 25ns w.r.t. the TLU trigger.

3. Registers

The *Firmware Register* should read x'FD9A' - acknowleding that a NIM I/O mezzanine is plugged to port F and that the firmware version 9.A is loaded.

The *Status Register* allows to set the TLU VETO mode (bit 1 = '1'), the handshake mode (bit 4 = '0' ➞ 'Trigger Data Handshake', else 'Simple Handshake') and to choose the signal inputs:

- Bit 8 = '0' ➞ all handshake signals are received on LVDS port A, see table 2 for channel assignment.
- Bit 8 = '1' ➞ the TRIGGER signal is received on NIM port G(0), the TRIGGER_DATA are received on NIM port G(1) - this is a test mode.

Bits 12…14 of the *Status Register* are intended for selftest purposes - see chapter 4.

Writing a '1' to bit 2 of the Status Register resets the module.

From the *Trigger Register* the READY status may be read (bit 1).

Firmware Register coding *ReadOnly*
addr: x"100C"

bits 15...13	12...10	9...7	6...4	3...0
IDD	IDE	IDF	Demo	Version

Status Register coding *Read-Write*
addr: x"1000"

bits 7…5	4	3	2	1	0
n/a	Hand shake	n/ a	Reset	Veto	n/a

bits 15	14…12	11…9	8
n/a	Test	n/a	Port select

Trigger Register Coding *ReadOnly*
addr: x"1004"

bits 15...4	3	2	1	0
n/a	Done	Busy	Ready	Latched Trigger

Pattern Register Coding *ReadOnly*
addr: x"1008"

bits 15	14...0
n/a	Trigger Number

Table 1

4. Channel Mapping

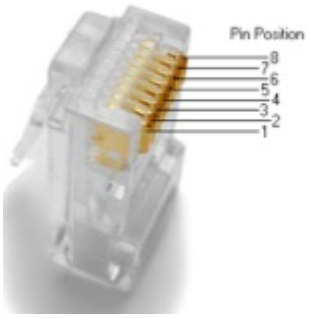
The LVDS TLU interface (when bit 0 of the *Status Register* is set to '0') uses port A of the V1495 module for the signals driven by the TLU and port C for the signals sent to the TLU. See table 2 for channel assigment!

In the Test mode (*Status Register* bit 8 = '1') the NIM outputs G(0) and G(1) are assigned different signals. Especially at the F(7) output a fake trigger is provided with an adjustable frequency between ~10Hz and ~600Hz (depending on the setting of bits 13 and 14 of the *Status Register*). It may be directly connected to input G(0) for selftest of the module.

Port Mapping

standard mode	*test mode*	*port channel*	*purpose*
TRIGGER/ TRIGGER DATA	n/a	A(16)	TLU Interface (LVDS)
BUSY		C(18)	
T_CLK		C(17)	
TRIGGER NUMBER		C(14...0)	
and others...			
	TRIGGER	G(0)	Test (NIM)
	TRIGGER DATA	G(1)	
Clean TRIGGER	TEST	F(7)	
Clean TRIGGER	Latched Trig.	F(6)	
Clean TRIGGER		F(5)	
Clean TRIGGER	DONE	F(4)	
READY		F(3)	
BUSY		F(2)	
T_CLK		F(1)	
TRIGGER (copy)		F(0)	

Table 2



Cable Wires

nb.	*color*	*pin*	*purpose*
1	acc.red	C38	T_CLK-
2	red	C37	T_CLK+
3	acc.green	C40	BUSY-
4	blue	C39	BUSY+
5	acc.blue	A38	RESET-
6	green	A37	RESET+
7	acc.brown	A36	TRIGGER-
8	brown	A35	TRIGGER+

Table 3