Tests of Silicon Strip Modules for the Upgrade of the ATLAS Detector at the LHC

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Abstract

The ATLAS experiment at the Large Hadron Collider (LHC) will be upgraded. For the upgrade of the semiconductor Tracker (SCT) a custom readout system is being used. In this thesis parts of the corresponding data acquisition software and database systems are tested and modified to fulfill the needs of the upgrade.

The main works of this thesis are:

1.) to evaluate the test routines in SCTDAQ and study the results;

2.) to establish the local database system;

3.) to achieve the goal of stable and noise-reduced readout system.

The readout system is based on a high-speed input/output (HSIO) board. An HSIO based readout system is available at DESY (Zeuthen site). The SCTDAQ and HSIO based readout system tests and calibrates the performance of the device under test. In order to get useful and comparable test results within SCT community, it is critical to make the readout system stable and with as little noise as possible. For the future mass production of silicon strip modules of end-caps, the local database is established to record the information of each module so that it can be accessed easily through a web front end.

Acknowledgements

If I could experience any joy of the study and research of physics, I appreciate whoever I knew is also enthusiastic about it. Because when I encounter any frustration in researching, it reminds me I am not alone. The sun arises after darkness.

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Chapter 1

The Large Hadron Collider and the ATLAS experiment

*There is nothing new to be discovered in physics now. All that remains is more and more precise measurement. . . . Beside two little dark clouds on the clear blue sky of physics.**

— Lord Kelvin, Nineteenth-Century Clouds over the Dynamical Theory of Heat and Light

1.1 Open Questions in Fundamental Physics

The scientific purpose of the LHC (Large Hadron Collider) is to explore the inner structure of matter and the forces that govern its behavior, which include testing for the existence of the hypothesized Higgs boson and of new particles predicted by supersymmetry. The LHC and its four detectors, ATLAS (A Toroidal LHC ApparatuS), CMS (Compact Muon Solenoid detector), LHCb (Beauty Experiment), ALICE (A Large Ion Collider Experiment) are designed to answer some of the fundamental open questions nowadays in physics. [1]. Four of these unsolved questions to be investigated at the LHC are:

1.1.1 The origin of mass

According to the standard model, elementary particles (six quarks and six leptons) are held together by the gauge bosons (the electromagnetic force is mediated by photon, the weak force by $W^{\pm}$- and Z^0- bosons and the strong force by eight gluons) to construct all the matter. It is still unclear through which fundamental mechanism particles acquire mass and

*These two clouds (ether + ultraviolet catastrophe) turned out to bring the new physics of the 20^{th} century: the theory of relativity and quantum mechanics.

why there is such a large difference between the particle masses. One of the favored theories predicts the existence of a Higgs boson which mediates the process that gives mass to the other particles. If the Higgs (standard model Higgs) exists, its mass is expected to be within a range of approximately 113 GeV and 850 GeV. [1] This energy range is covered by the LHC and the multipurpose detectors, ATLAS and CMS, which are designed to give a definite answer on the existence of the Higgs.

1.1.2 Dark matter and dark energy

About 96% of the universe are composed of dark matter and dark energy, which are not ordinary baryonic matter. The energies involved in proton-proton collisions at the LHC will be similar to those in particle collisions in the first trillionth of a second after the Big Bang. The LHC experiments with the ATLAS and CMS detectors will help us to understand the thermal history of nucleosynthesis and search for supersymmetry particles which are predicted to be a possible candidate for the dark matter. [3]

1.1.3 Matter-antimatter asymmetry

The annihilations of matter and antimatter would have left the universe with only photons, if there would exist a perfect symmetry between them. But apparently the visible universe is dominated by matter and this violation of the symmetry between matter and antimatter is to be studied by the LHCb experiment. LHCb is designed to efficiently detect B-mesons (which consist at least one b quark or antiquarks) and the products of their decays. The accurate measurement of charge parity violation, which explains the matter and antimatter violation, can be studied in different B-mesons decay channels. [1]

1.1.4 The quark-gluon plasma

By colliding beams of lead ions, the LHC will be able to produce a state of matter which existed a few millionths of a second after the Big Bang. The ALICE detector is designed to investigate the nature and properties of the quark-gluon plasma, which is believed to have existed at that time.

1.2 The Large Hadron Collider

The Large Hadron* Collider was built by the *European Organization for Nuclear Research* (CERN) to test various predictions of high-energy physics. It lies in a tunnel, 27 km in circumference, and up to about 175 m beneath the Franco-Swiss border near Geneva, Switzerland. The LHC is designed to collide two opposing beams of protons at a momentum of 7 TeV per particle or of lead nuclei at 574 TeV per nucleus. In the following, the focus will be on the case of proton-proton collisions which are mainly studied in the ATLAS experiments. Protons are created in an ion source called a Duoplasmatron. These protons are preaccelerated in the LINAC2 (LINear ACcelator), the booster, the PS (Proton Synchrotron) and the SPS (Super Proton Synchrotron) before being injected into the LHC accelerator and storage ring, as shown in Fig. 1.1.

In order to force the 7 TeV protons on a circular orbit within the beam pipe, a magnetic field of 8.33 T is needed. The field is generated by the superconducting magnets (Nb-Ti) with a working temperature of 1.7 K which is obtained by cooling the magnets with superfluid helium. The proton beams are discontinuous and bundled into a maximum of 2808 bunches with 10^{11} protons each [5]. The current designed bunch crossing rate is 25 ns.

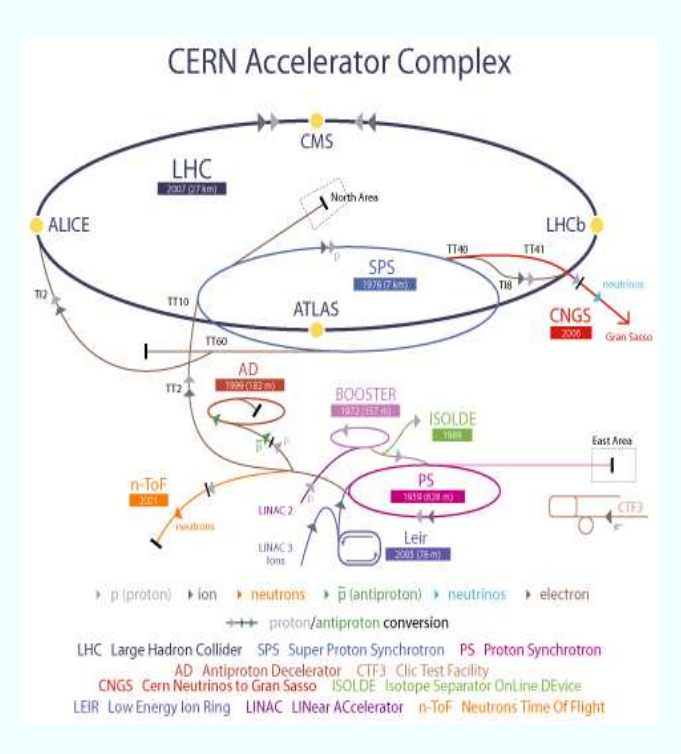


Figure 1.1: The LHC Injection Chain [7]

The current designed luminosity of the LHC is 10^{34} cm^{-2}s^{-1}. In the future, the LHC will be able to provide a designed luminosity up to 5×10^{34} cm^{-2}s^{-1}. Details about the designed luminosity and the upgrades will be discussed in Chapter 2.

*"Hadrons" refers to particles composed of quarks.

1.3 The ATLAS detector

ATLAS is a "onion type" detector with cylindrical and forward-backward symmetry with respect to the interaction point, as shown in Fig.1.2. Each subdetector is designed to perform a specific task. The purpose is to identify and to precisely measure the energies and momenta of all the particles produced in the proton-proton collisions. [9] The subdetectors from inside to outside are Inner Detector, Calorimetry and Muon Spectrometer.

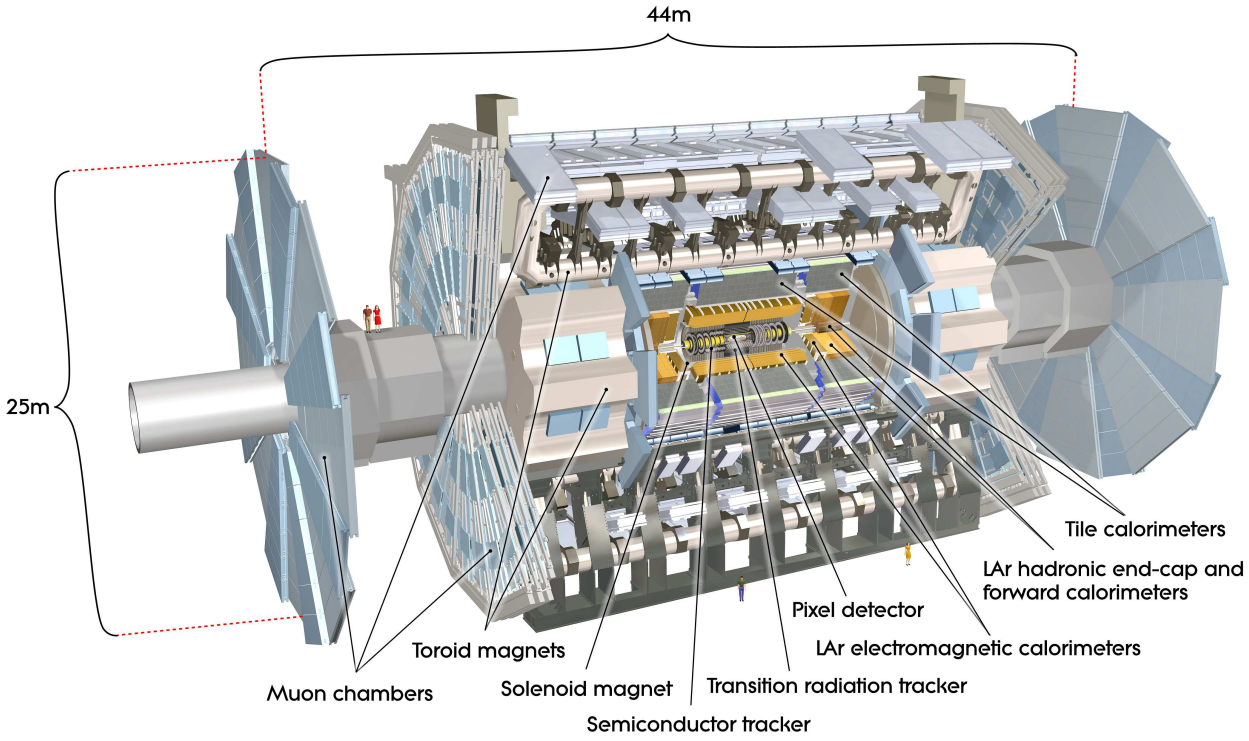


Figure 1.2: Cut-away view of the ATLAS Detector [6]

Prelude to Design :

The Coordinate System

A special coordinate system is used within ATLAS:

The origin is at the nominal interaction point.

The z (longitudinal) axis points along the beam pipe.

r (transverse) is the axis perpendicular to the beam pipe.

ϕ is the azimuthal angle around the beam pipe.

θ is the angle of a particle track with respect to the beam pipe [12].

The coverage of the detector can be described by pseudorapidity, η. [9]

$$\eta = -\ln\left(\tan\frac{\theta}{2}\right) \tag{1.1}$$

1.3.1 The Magnet System

Prelude to Design :

Charged particles follow spiraling trajectories in the magnetic field. We can measure the momenta of these charged particles from the curvature of their trajectories. Then the energies of these charged particles can be derived.

The choice of the magnetic field configuration defines the basic detector design. Two typical magnet configurations are solenoidal and toroidal, which respectively generate parallel and perpendicular magnetic fields relative to the beam axis.

Solenoid for the Inner Detector

The central solenoid provides an axial magnetic field of 2 T for the Inner Detector. In order to place the central solenoid in front of the LAr electromagnetic calorimeter and to achieve the desired calorimeter performance, careful minimization of material is required. To avoid two vacuum walls, the central solenoid and LAr electromagnetic calorimeter are placed into a single common vacuum vessel.

Toroids for the Muon Detector

The toroidal magnetic field for the muon spectrometer is generated by three air-core toroids (two end-cap toroids and one barrel toroid with magnetic fields of 1 T and 0.5 T respectively).

1.3.2 Inner Detector

Prelude to Design :

The Inner Detector (ID) is used to measure the trajectories of charged particles emerging from the LHC collisions. The ID is designed to provide excellent momentum resolution for charged particles, primary and secondary vertices* for charged particles above a given threshold of the transverse momentum p_T and the sign of the electric charge.

The particle flux decreases from the particle source, varying from hit rates of $10^8 \mathrm{cm}^{-2}\mathrm{s}^{-1}$ at a radius of $r = 50.5$ mm (innermost layer of the Pixels); to 5×10^6 $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at $r = 299$ mm (innermost layer of the SCT); and 5×10^5 $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at $r = 1000$ mm (end of TRT), as shown at Fig. 1.3.

*The position where a particle produced in a collision further decays into a new set of particles.

The layout of the Inner Detector, as shown in Fig. 1.4, covers the pseudorapidity (see Equ. 1.1) region $|\eta| < 2.5$.

Pixel Detectors There are three layers of silicon pixel detectors which provide the highest detection granularity in the innermost part of ATLAS. The pixel sensors are 250 μm thick silicon detectors using oxygenated n-type wafers with readout pixels on the n^+-implanted * side. The nominal pixel size is 50×400 μm^2 resulting in an estimated particle occupancy† of 10^{-4} per pixel and LHC bunch crossing. There are 47232 pixels on each sensor, 1744 pixel sensors in total, and hence approximately 80 million readout channels readout channels. [9] [13]

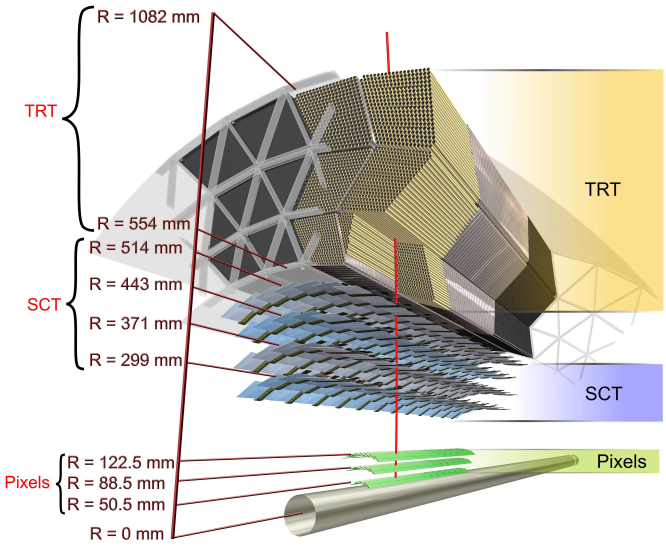


Figure 1.3: ATLAS inner tracking system [6]

Semiconductor Trackers (SCT) In the intermediate radial range of the ID reside the SCT silicon microstrip detectors. There are four cylindrical double layers of silicon microstrip sensors. A silicon microstrip layer consists of two single-sided p-in-n sensors glued back to back (one axial and one with 40 mrad stereo angle) with AC-coupled readout strips. Each sensor has 784 strips with an 80 μm pitch, and there are 15912 sensors in total. The strip pitch was determined by the required digitising precision, granularity, particle occupancy and noise performance. The sensor thickness of 285±15 μm is a compromise between the required operating voltage, the primary signal ionisation and the simplicity of fabrication. To maintain an adequate noise performance after degradation due to radiation damage, the silicon sensors (both of pixel detectors and SCT) must be kept at low temperature to keep the leakage current low (approximately –5 to +10^{o}C), details shows in Chapter 2.3.1.

Transition Radiation Tracker (TRT) In the outermost region of the ID, the transition radiation tracker is used, which consists of gaseous straw tube detectors. There are on average 36 axial straws (which means each track transverses approximately 36 axial straws) of 4 mm diameter contained in the barrel TRT modules within their support structure. Each straw

*The n^+-implants allow the detector to operate with good charge collection efficiency after type inversion, even below the depletion voltage, because the depletion zone grows from the pixel side.

†Particle occupancy is the average fraction of collisions in which a signal channel register a signal

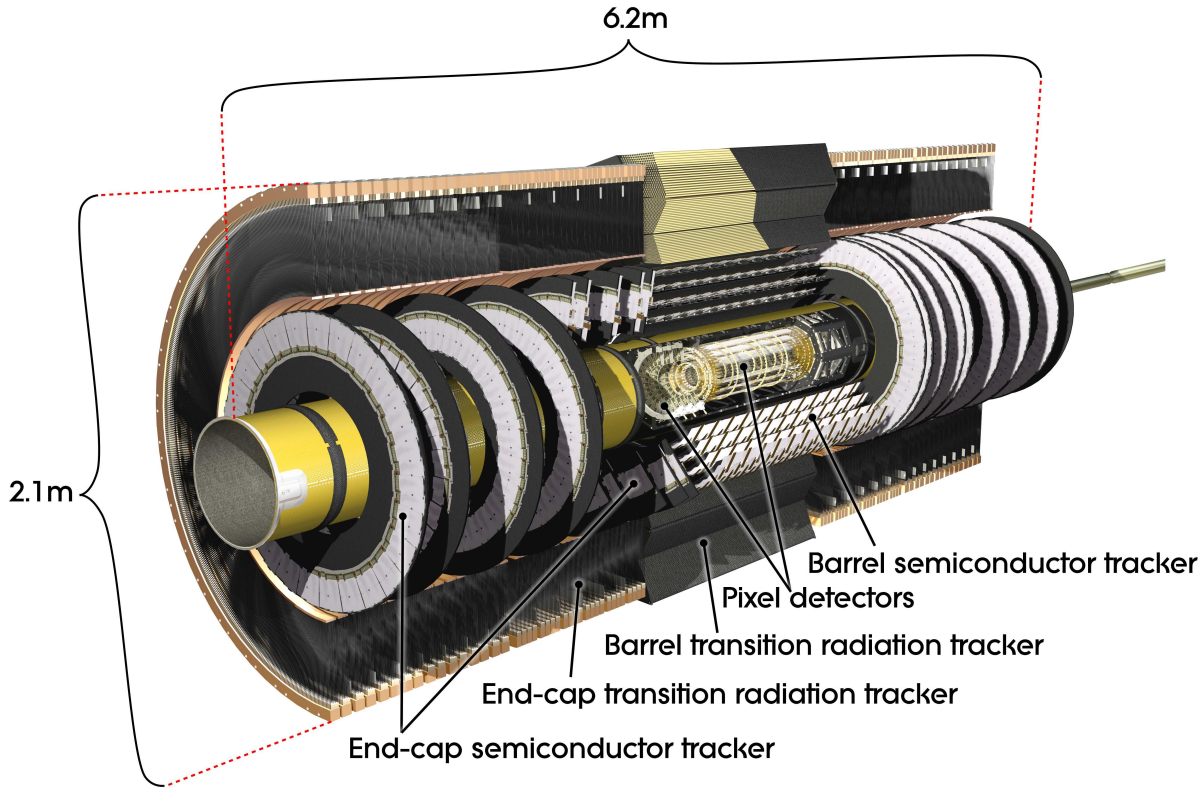


Figure 1.4: ATLAS Inner Detector [6]

is a small cylindrical gas-containing chamber, with an anode wire in the center, and the wall of straw acting as a cathode. The straw is filled with Xenon-based gas mixture. Apart from tracking, the TRT is capable of identifying particles.

1.3.3 Calorimetry

Prelude to Design :

Outside the Inner Detector, the next layer are the sampling calorimeters*, which are used to measure the energies of the incident particles. The principle of calorimetry is: the incident particle interacts with a shower material or absorber and produces a shower of secondary particles. The calorimeters must provide good containment for electromagnetic and hadronic showers, and also limit punch-through, which means particles leaking out of the calorimeter, into the muon system. Thicker calorimeters improve the punch-through effects of the detector.

*Sampling calorimeter made of alternating layers of passive(absorber)/active(dececter) materials.

Electromagnetic Calorimeter The electromagnetic calorimeter is a lead/liquid-argon (LAr) detector covering the pseudorapidity region of $|\eta| < 1.475$ for the barrel and $1.375 < |\eta| < 3.2$ for the two end-caps. When high-energy electrons or photons pass through the lead, an electromagnetic shower is produced whose intensity is proportional to the incident energy. The active material, argon, is ionized by the shower and produces a current which is also proportional to the energy of the incoming particle.

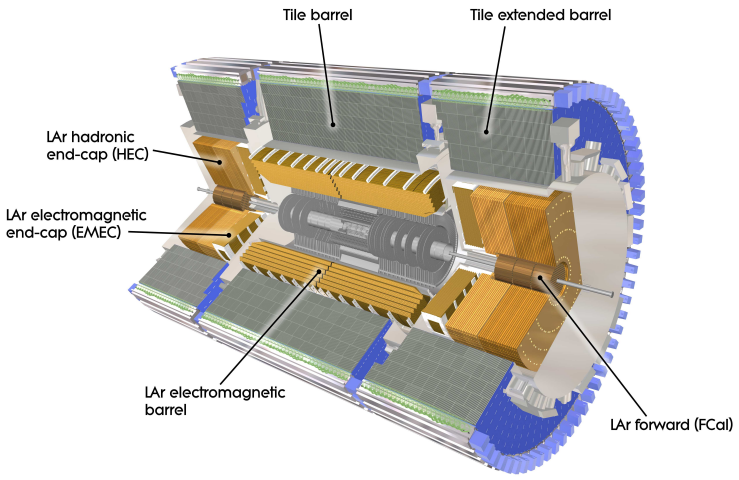


Figure 1.5: ATLAS Calorimetry [6]

Hadronic Calorimeters The two main functions of the hadronic calorimeters are: 1. To measure the energies and directions of jets, the clusters of particles, which result from the hadronization of quarks or gluons. 2. To detect the missing transverse energy ($E_{\mathrm{T}}^{\mathrm{miss}}$) produced by undetectable neutral particles, by monitoring the total transverse energy flow. In ATLAS, there are three different types of hadronic calorimeters:

- Tile* Calorimeter
- Hadronic End-cap Calorimeter (HEC)
- Forward Calorimeter (FCal)

1.3.4 Muon Spectrometer

Prelude to Design :

The standard model predicts that the Higgs boson decays into two Z bosons, each of these can, in turn, decay into a pair of muons. The Muon spectrometer is designed to identify, trigger and accurately measure the momenta of muons. A high magnetic field is necessary for good muon momentum resolution and triggering capability. The Muon Spectrometer is the outermost part of ATLAS detector and contains four main parts.

*Scintillating plastic plates

Monitored Drift Tube Chambers (MDTs)
The monitored drift tube chambers measure the precise track coordinates which are required to get the momentum in both barrel and end-cap regions.

Cathode Strip Chambers (CSCs)
The cathode strip chambers complement the higher pseudorapidity region of MDTs.

Resistive Plate Chambers (RPCs)
Resistive Plate Chambers up to pseudorapidity region $|\eta| < 2.4$ are used in the barrel region as the trigger system to select events with muon candidates.

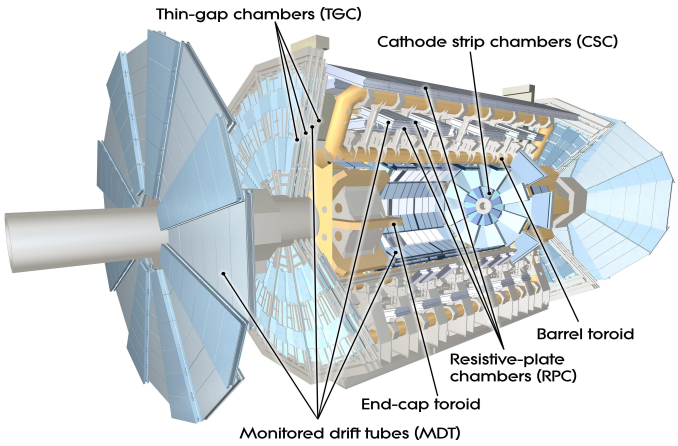


Figure 1.6: ATLAS Muon Spectrometer [6]

Thin Gap Chambers (TGCs)
Thin Gap Chambers are the trigger chambers used in the end-cap regions where they have to sustain higher rates.

1.3.5 Trigger and Data Acquisition

Prelude to Design :

At the bunch crossing rate of 40 MHz and an average of 23 inelastic proton-proton interactions per bunch crossing, raw data is generated at a rate of 60 TB/s while the rate for event storage is 200 Hz (the average event size is around 1MB) [1]. The online data acquisition system must reduce the rate of incoming raw data by at least three orders of magnitude.

Therefore a trigger system is needed to select all good event candidates, reject most of the background events and be flexible for new physics [4]. The Data Acquisition System (DAQ) is responsible for buffering the event data from the readout electronics at the level 1 trigger accept (L1A) rate. The ATLAS trigger system has three levels, level 1 trigger, level 2 trigger and event filter.

Level 1 Trigger (L1)

The L1 trigger is implemented using custom-made electronics. They implement algorithms to search for signatures from high-p_T muons, electrons/photons, jets and τ-leptons decaying into hadrons. The L1 Trigger also selects events with large $E_{\mathrm{T}}^{\mathrm{miss}}$ and large total transverse energy. The detector readout system works in two steps:

1. L1 accepts events, sends L1A (Level 1 Accepted). The maximum L1A rate is 75 kHz.
2. define the region of interest (RoI).

The L1 decision must reach the front-end electronics within 2.5 μs after the bunch-crossing time.

Level 2 Trigger (L2) and **Event Filter (EF)**

The L2 and EF together form the High-Level Trigger (HLT), which is based on commercially available computers and networking hardware. The L2 trigger uses the Regions-of-Interest (RoI) from L1 to limit the amount of data transferred from the detector readout. The EF uses offline analysis procedures on fully-built events to further reduce the event rate which then is recorded for subsequent offline analysis.

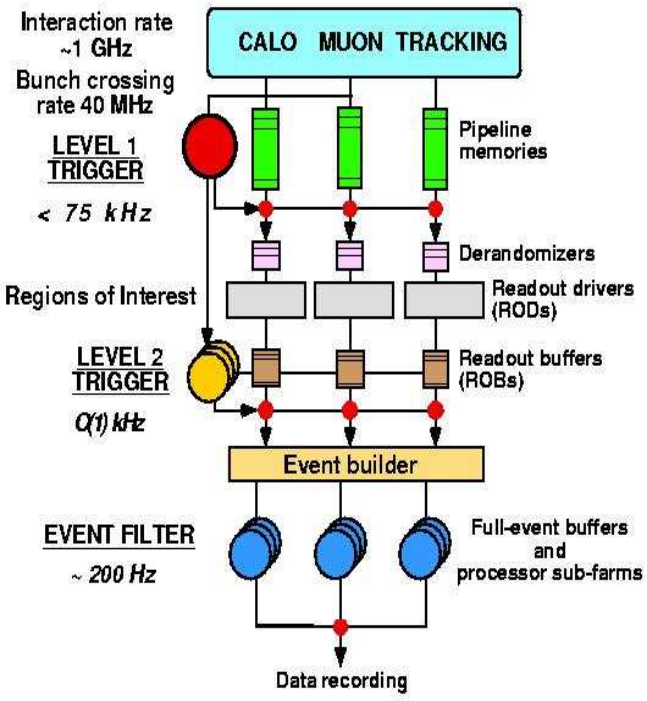


Figure 1.7: Block diagram of the ATLAS Trigger system [8]

Chapter 2

Upgrade of the ATLAS Tracker Detectors

2.1 Motivation

The LHC has been operated since September 2008, and is expected to reach an integrated luminosity of several hundred fb^{-1} of proton-proton collisions per experiment in ten years [14]. To either discover or exclude the Higgs boson (or an alternative mechanism up to the TeV range), more studies with extended statistics will be needed. If SUSY particles are found, it is necessary to measure their decay chain for identifying their structure. The statistics of the current LHC will be too low for these purposes.

The goal of the upgrade of the LHC and the ATLAS detector is to reduce the statistical errors and replace the radiation damaged sensors with newly designed detectors to cope with the high luminosity at the High-Luminosity LHC (HL-LHC). The luminosity upgrade can increase the physics potential to extend the mass reach, improve the precision of the measurements and increase the sensitivity to rare processes [26].

A higher luminosity of the upgraded LHC will cause higher occupancies of the detectors and higher radiation. Therefore it is necessary to upgrade the detector to get higher granularity of detection, to improve the radiation hardness, and to introduce new powering schemes to account for the number of increasing electronic channels due to the higher granularity of the detector.

2.2 Evolution from LHC to HL-LHC

Prelude to Design :

The Designed Luminosity

N_b, the number of particles per bunch (1.15×10^{11}) ;

n_b, the number of bunches (2802) ;

f_r, the revolution frequency ($1.12 \times 10^4 \mathrm{s}^{-1}$) ;

γ, the relativistic factor (7461) ;

ϵ_n, the normalized emittance (3.75×10^{-4} cm rad) ;

β^*, the beta value at the interaction point (55 cm) ;

F, the reduction factor due to the crossing angle (0.86) [14]

$$L = \frac{N_b^2 n_b f_r \gamma}{4\pi\epsilon_n \beta^*} F \tag{2.1}$$

With the designed values within the parentheses of each parameters, the nominal value of the instantaneous luminosity of the LHC is : 1×10^{34} cm^{-2}s^{-1}.

Two phases of upgrade towards the HL-LHC are planned :
PHASE-I: Replacing the inner triplet focusing magnets and the first stage proton linac during 2013–2015.
PHASE-II: Two new accelerators to be built from 2017. The number of particles per bunch (N_b) and the beta value at the interaction point (β^*) are the major parameters to be upgraded. [14] Therefore the machine upgrade consists of improved beam focusing by reducing the β^* and increasing the beam currents. [26]
The goal is to increase the peak luminosity from 1×10^{34} cm^{-2}s^{-1} up to 5×10^{34} cm^{-2}s^{-1}.

2.3 Evolution of ATLAS Tracker

Two challenges need to be overcome for the design of the detectors to cope with the HL-LHC.
1. **pile-up events**:
Pile-up event per bunch crossing will increase from ∼23 * up to ∼200 [29].
2. **radiation damage**.
The detectors at low radii r and large pseudorapidity η are mostly affected by the harsher radiation environment and higher detector occupancies. Therefore the ATLAS detector upgrades

*23 pile-up event means that there are 23 separate collisions occurred when two bunches of LHC protons crossed each other inside ATLAS.

focus on the Inner Detector, forward calorimeter and forward muon wheels. [27] Increased radiation hardness of new detector electronics and higher bandwidth of the readout system (to deal with the coming higher detector granularities and occupancies) are also concerned in the upgrade plans.

For the study of this thesis, the focus is lies on the upgrade of the semiconductor tracker (especially of the silicon strip tracker) in the Inner Detector. Within the ATLAS upgrade plan, the Inner Detector will be replaced entirely by an all-silicon system. [28]

The reason to replace the entire ID is that the Transition Radiation Tracker at larger radii will suffer from a prohibitively large occupancy. Furthermore the Semiconductor Tracker and Pixel Detectors at smaller radius will get reduced performance by radiation damage of the sensors and the front-end electronics.

One of the consequences of replacing the TRT with silicon is the loss of its neutron-absorbing properties [27].

The current baseline layout of the Inner Detector upgrade is shown in Fig. 2.1.

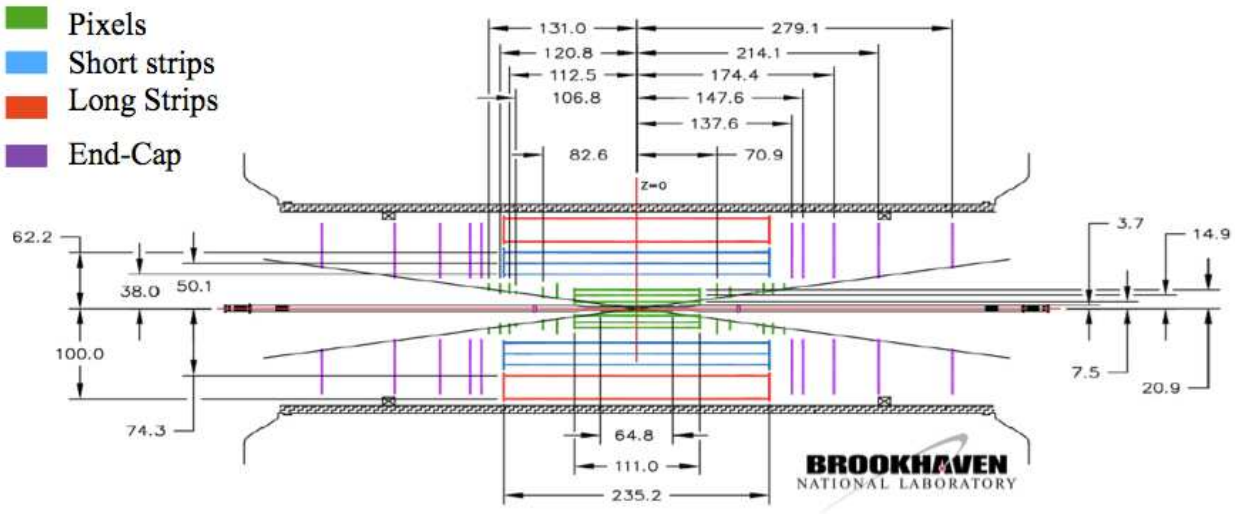


Figure 2.1: Current Strawman Layout of the Upgrade ID [19]

There will be four pixels layers (innermost) and five strip layers, three inner layers with short strips (length of 2.48 cm) and two outer layers with long strips (length of 4.8 cm), in the central barrel region. The forward region is covered by six pixel and five strip disks on either side. [29]

2.3.1 Silicon Strip Tracker Upgrade

Theory of Semiconductor Detectors

Semiconductor detectors consist of single crystals of semiconductor (silicon is used in ATLAS), to which a voltage is applied between two attached electrodes, see Fig. 2.2. The device operates like a solid ionization chamber. Electron-hole pairs are created when ionizing particles cross through the crystal. An applied electric field makes the electrons (holes) in the conduction (valence) band move through the crystal at their mobility. The time to collect holes at room temperature across 0.5 mm of silicon with a typical voltage gradient of 5 kV/cm^{-1} is about 20 ns, in the use of the data of Table 2.1.

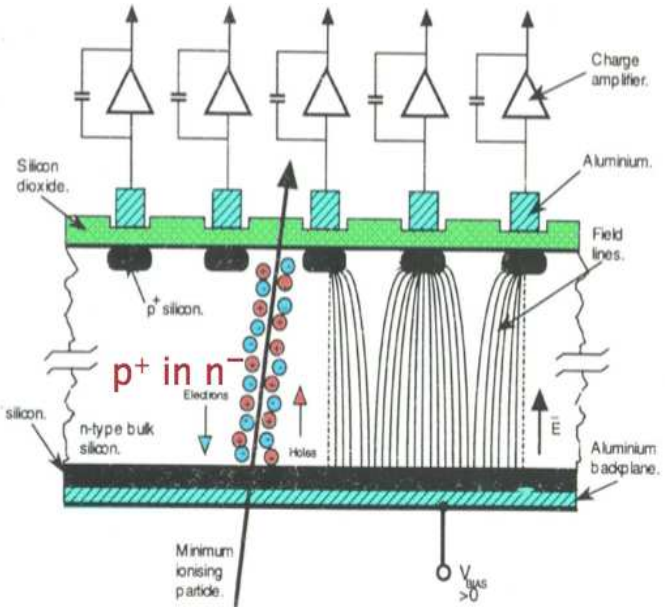


Figure 2.2: Cross-section of a Silicon Strip Detector and Representation of Signal Formation [30]

The concept of p-n junction detectors is used in the ATLAS strip tracker. When extra electrons from the donor (n-type) material migrate to combine with acceptors, holes, in p-type material, a depletion region is formed in a p-n junction. The depleted zone is the region of the detector sensitive to radiation.

Table 2.1: Physics Properties of Silicon [31]

Working Temperature (K)	Electron Mobility ($cm^2V^{-1}s^{-1}$)	Hole Mobility ($cm^2V^{-1}s^{-1}$)	Energy per Electron-Hole Pair (eV)
300	1350	480	3.62
77	21000	11000	—

By applying an external voltage in the reverse bias direction, the depleted zone can be made deeper. Reverse bias not only increases the electric field in the depletion zone but also increases the rate and efficiency of electrons and holes collected at the electrodes. But it also gives rise of a small current, leakage current, which contributes to electronic noise and a consequent degradation in the signal-to-noise ratio of the output pulse. [31]

2.3.1.1 Silicon Sensors

The Current Setting :

p-in-n Sensors

The sensors of the SCT use single-sided p-in-n technology with AC-coupled readout strips. Depending on the sensor position, the integrated luminosity and the length of warm-up periods, the operating voltages of the sensors can reach up to 250 to 350 V.

The thickness of sensor ($285 \pm 15\mu$m) is a compromise between the required operating voltage, the primary signal ionisation and the simplicity of fabrication. In order to achieve the required digitising precision, granularity, and noise performance, the strip pitch is 80 μm. [9]

Candidates of Upgrade :

ATLAS07

The n-in-p sensors are chosen to be the future upgrade silicon strip sensors. For the n-in-n and n-in-p sensors, the signals are transferred by electrons to the strips. For p-in-n sensors, holes transfer the signals. Electrons in silicon travel three times faster than holes, see Table 2.1. To cope with HL-LHC, faster signal transfer is needed.

Type inversion of silicon can be a result of radiation damage. For n-in-n sensors, the deposited charge can always reach the electrode and the sensors can work under-depleted. There is no type inversion for n-in-p sensors and the sensors can also work under-depleted. But for current p-in-n sensors, the deposited charge can not reach the strips if the sensor is under-depleted. To conclude the pro and con of these three type sensors, the n-in-p and n-in-n sensors are better choices than p-in-n sensors. To compromise with the price, the n-in-p sensors is chosen (n-in-n is around twice expensive than n-in-p). [33] [14]

2.3.1.2 Readout ASIC

The Current Setting :

ABCD3TA

ABCD3TA (ATLAS Binary Chip) is a 128-channel ASIC with binary architecture for the readout of silicon strip detectors based on CMOS devices. [32]. There are several blocks of the readout chip which have different functionality to readout and process the signals and commands. The Front End block, as shown in left upper corner of Figure 2.3, accepts the input signals, applies the threshold voltages from an internal digital-to-analogue-convertor (DAC), corrects the threshold after trimming and calibrates the strobe signals and the timing. The signals are delivered by the preamplifer-shaper with peaking time 25 ns. A discriminator with a common threshold follows the preamplier-shaper circuit and is controlled by an internal 8-bit DAC. In order to correct threshold offsets and keep threshold to a common value, a

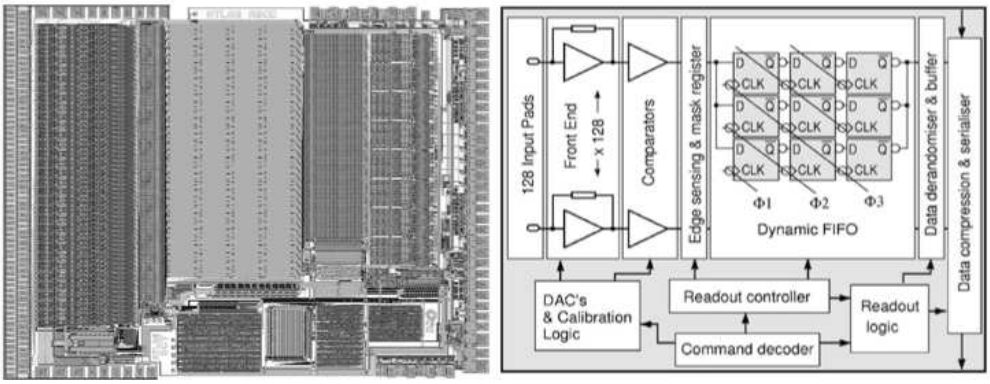


Figure 2.3: The left figure is the layout drawing of the ABCD3TA, and the right one shows its block diagram. [32]

4-bit TrimDAC is used.

The mask register block in located in the middle of the readout chip, which masks the channels can not be trimmed, details in Chapter 3.3.4.

Candidates of Upgrade :

ABCN25 (or coming ABCN13)*

Two challenges to be overcome in the readout ASIC for the upgrade are power consumption of nearly 70 million readout channels and the large amount of data which needs to be transfered. The ABCN25 (ATLAS Binary Chip Next) architecture follows the concept of ABCD3TA, but uses a different token mechanism, additional configuration commands and register read-back protocols and a more radiation tolerant layout. [35]

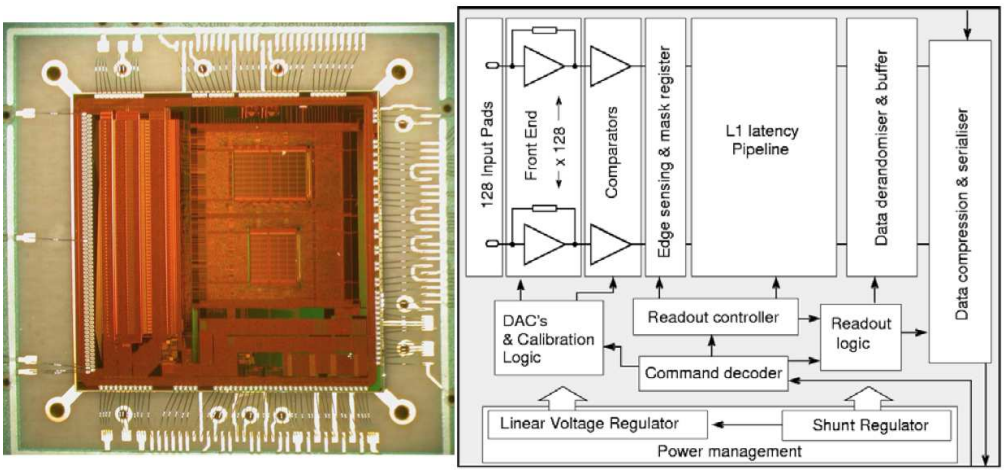


Figure 2.4: The left figure is the photograph of the ABCN25, and the right one shows its block diagram. [34] [35]

*The number of 25 or 13 after ABCN refers to the readout ASICs in 250 nm or 130 nm CMOS technology.

To solve the power distribution problem, ABCN25 comprises two prototypes of distributed shunt regulator circuits that can be used alternatively [36]. To deal with the huge amount of data, the Pipeline and Readout Buffer blocks of the ABCN25 are used to write and store the clock information and data corresponding to each L1 trigger being sent.

2.3.1.3 Hybrid & Module

The Current Setting :

SCT module

A barrel SCT module consists of four sensors, two on the top side and two on the bottom side. They are glued back to back on a thermal pyrolitic graphite base board which provides thermal and mechanical support structure. The sensors are rotated with their hybrids by ±20 mrad around their geometrical center, to provide a stereo hit information. There are six ABCD3TA readout chips on each side of the module.

For fully irradiated modules, a noise occupancy per channel of $< 5 \times 10^{-4}$ for a threshold of 1 fC is specified.

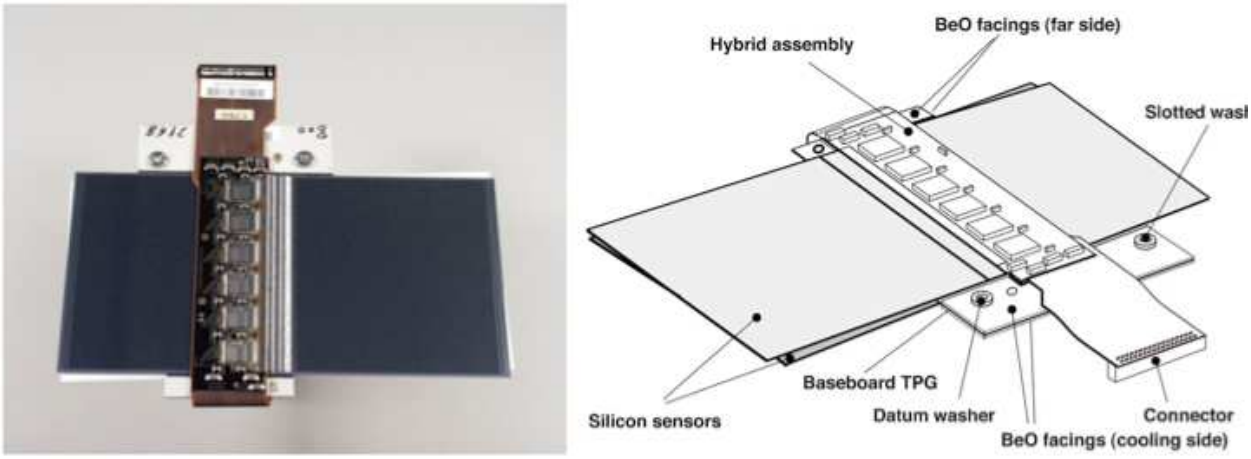


Figure 2.5: The left figure is the photograph of current SCT module, and the right one is the sketch of the module [9].

Candidates of Upgrade :

Stave (baseline design)

The stave concept is the baseline integration layout of sensors, cables and cooling system, see left side of Figure 2.6. Single-sided modules are mounted on both side of a common support structure. Twenty readout chips are placed on each of two flex circuits (hybrids) which themselves are glued directly onto a sensor to form a module. The modules are glued onto the bus cables, which is laminated onto the cooling and support structure [37].

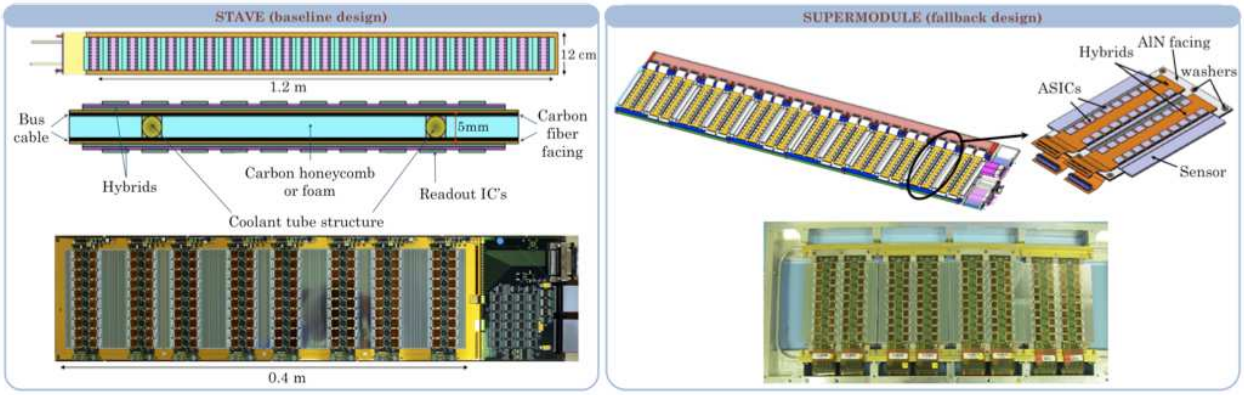


Figure 2.6: The left figure is Stave module, and the right one is the Supermodule. [19]

Supermodule (alternative choice)

The supermodule concept follows the current SCT module design. The sensors are glued on thermal pyrolitic graphite base boards. The hybrids are glued on heat conducting carbon-carbon bridge to transport the heat to the module edges. [37]

2.3.1.4 Readout System & DAQ

The Current Setting :

VME Units

VME * units include five main parts: [24]

1. MuSTARD (Multi-channel Semiconductor Tracker ABCD Readout Device) to receive, store and decode data from the module.
2. SLOG (SLOw command Generator) to generate slow commands which control and configure the ATLAS SCT front-end chips.
3. CLOAC (CLOck And Control module) to generate the clock, fast trigger and reset commands for the SCT modules while running in stand-alone mode (in the absence of the global Timing, Trigger and Control system).
4. SCTLV (SCT Low Voltage power supply) to power the digital and analogue part of the chips ($V_{ddd} = 4.0$ V and $V_{dda} = 3.5$ V).
5. SCTHV (SCT high voltage power supply) to bias the modules detectors up to 500 V.

*A VME crate is used to provide a standard communication bus and hold several electronics modules. [10]

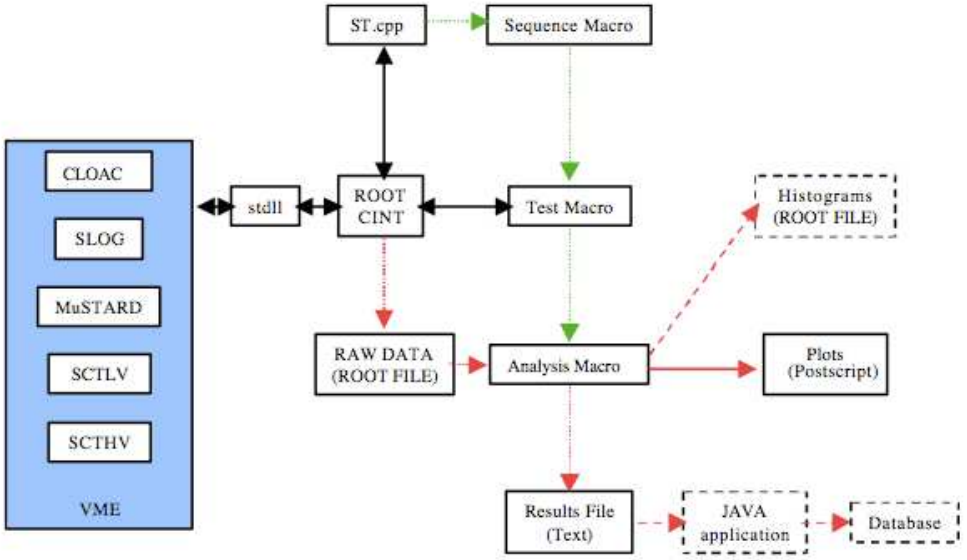


Figure 2.7: A schematic overview of the software components of SCTDAQ [39]

To perform electrical tests and to calibrate the readout and data acquisition, the SCTDAQ software is used. It is used within the SCT community for the standard data-acquisition. The top-level routines (STDLL) are written in C++ and ROOT for histogramming and analysis. The lower-level routines (STLIB, MuSTARD etc.) are written in C, which allows them to be used in the CERN Testbeam data-acquisition system. See the schematic overview in Fig. 2.7.

Candidates of Upgrade :

HSIO (default)

For the upgrade of ATLAS pixel and strip tracker, the High Speed Input/Output (HSIO) development board is intended to provide the signal processing capability. It can read out larger objects like Staves or Stavelet (Petals and Petallets), which the current VME units can not achieve. The HSIO board is a Virtex-4 FPGA (Field Programmable Gate Array) based stand-alone DAQ board which developed by SLAC. Many interface options like RJ45, gigE (gigabit Ethernet), SFP (small form factor

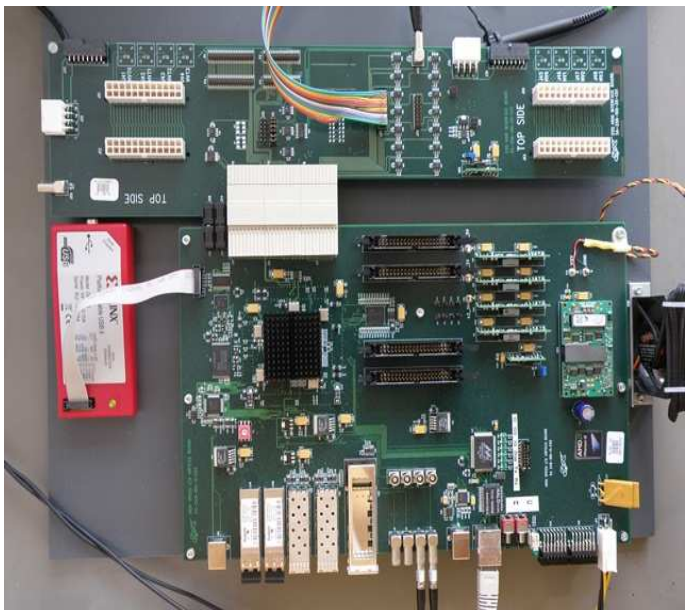


Figure 2.8: Photo of HSIO and Its Interfaceboard [23]

pluggable), XFP (10 gigabit small form factor pluggable) are available. USB connection is likely to be supported in the future. [40]
The software, SCTupDAQ, and HSIO firmware are under continuous development. The SCTupDAQ software is a modified version of SCTDAQ, written in C and C++. The HSIO firmware is written in VHDL (Very high speed integrated circuit Hardware Description Language). The detail of software development is discussed in Chapter 3.3.

SEABAS (alternative used to readout Supermodules)
SEABAS (Soi EvAluation BoArd with Sitcp) originally was used to readout the SOI (Silicon-On-Insulator) Pixel Detectors in KEK, Japan. The SEABAS readout board is also based on FPGA technology and provides an ethernet connection to the controller PC. But the man difference from the HSIO system is that two FPGAs are used in SEABAS, one user FPGA and another one called SiTCP (Silicon Transmission Control Protocol) FPGA. The user FPGA is for custom data-processing and the SiTCP FPGA is used for TCP/IP and UDP connection and I/O FIFO/registers [22].
The SEABAS readout software is written in C and the firmware written in Verilog [41].

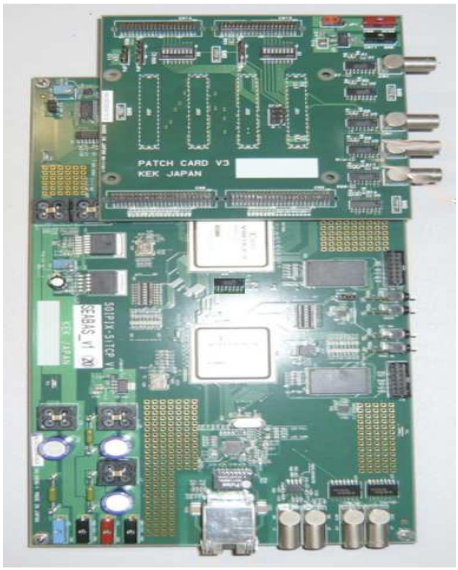


Figure 2.9: Photograph of SEABAS and Its Sub-board [22]

2.3.1.5 Powering

The Current Setting :
Independent Powering

Each of the current SCT detector modules has it own power cable. But for the upgrade to the HL-LHC, the independent powering is impossible to be applied on the modules due to the heavily increased number of channels [37].
Candidates of Upgrade :
In order to minimize the power loss in the cables and to transmit the power at higher voltage and lower currents, two main powering concepts are under studying.

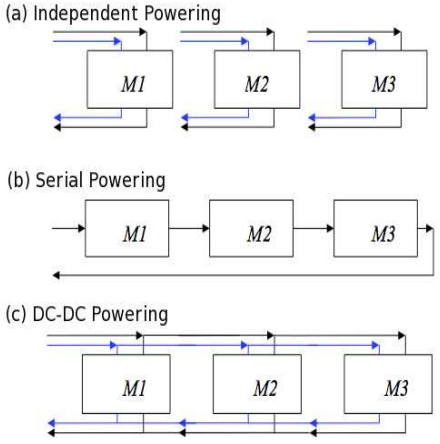


Figure 2.10: Powering Concept [20]

Serial Powering

Serial powering provides constant current to a chain of detector modules. The modules voltage is provided by shunt regulator and shunt transistor circuits on the modules. [37]

DC-DC powering

DC-DC powering distributes the power in the use of local DC-DC converters. Groups of modules are powered in parallel and local voltage step-down conversion is provided by buck converters. [37]

2.3.2 SCT Endcap Upgrade

The upgrade of the SCT endcaps mainly follows the Stave concept, but the major difference is the geometry. The structural elements of the future SCT endcaps are called "*petals*", like the petals of a daisy. 5 endcap disks comprise one full SCT endcap. One endcap disk is formed by 32 petals and with a diameter around 2 m. Each petal is based on a 650 mm long, 75 to 204 mm wide and 6 mm thick carbon fiber structure. [17]

As shown in Fig. 2.11, there are nine silicon modules per side (with nine different module geometries). As for the design concept of the Stave, the Petal comprises a light-weight core and carbon fiber facing on both sides. Metal cooling pipes are embedded into the core. The silicon detector modules are glued on both sides of the petals. [17]

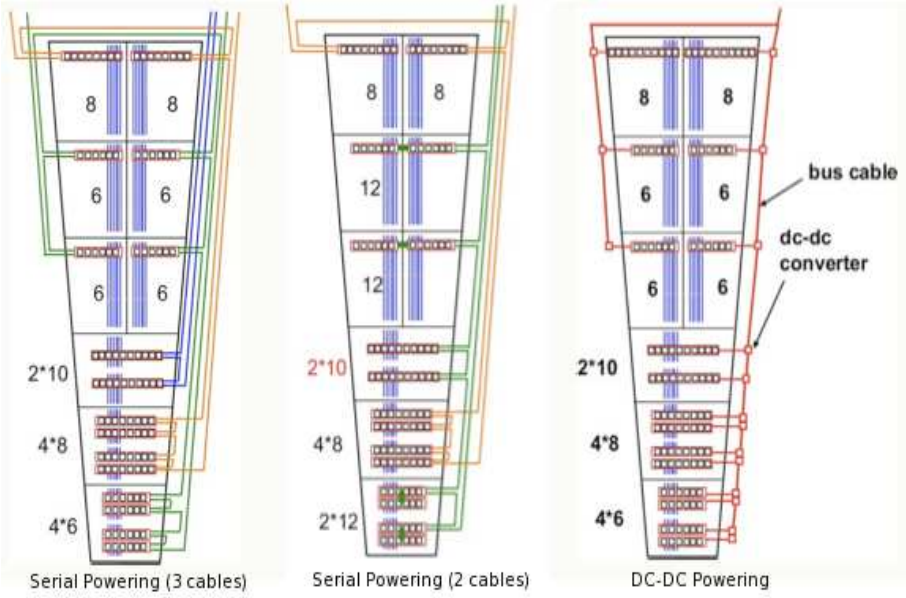


Figure 2.11: The schematic view of geometry and powering of petal [21]

Applying the powering concepts to the petal, the efficiency of DC-DC powering is higher than serial powering and results in lower total disk power. [21]

Chapter 3

Tests and System Setup of Silicon Strip Modules

For the upgrade of ATLAS silicon strip detector, the DESY ATLAS group mainly focuses on module production and the testing of sensor modules for the upgrade of the strip detector end-cap. This upgrade project is named "PETAL2014" [17].
The used read-out system and test procedures of devices under test are mainly discussed in this chapter. Three different devices (the single ABCN chip board, the single hybrid, and the dummy copper sensor module) were used to test the HSIO readout system. The setup and methods to test and analyze the module data are described in the following.

3.1 Silicon Strip Modules

3.1.1 Single Chip Board

The ATLAS ABCnext test board (as shown in Fig. 3.1) contains a single ASIC (ABCN25) and various LVDS (Low-Voltage Differential Signaling) drivers. Jumpers on the board enable the clock signal from the HSIO (bunch crossing clock) to be split into a data clock (clock for the data signals returned by the ABCN chip) and bunch crossing clock on the single chip board. The board needs to be powered with a main volt-

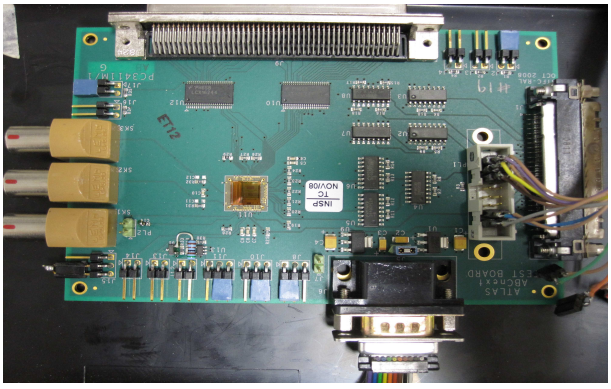


Figure 3.1: Single Chip Board

age of V=5 V, and analogue supply V_{dda}=2.2 V, and a digital supply V_{ddd}=2.5 V.

3.1.2 Single Hybrid

The single hybrid contains two columns of ABCN25 readout chips, each column consisting of 10 chips. Each chip has its specific wire bonding pattern to identify its address which is determined by a 7 bit binary code, shown in Table 3.1. The readout order can be defined by setting the "Master", "Slave" and "End'" chips of each column in a configuration file of the SCTDAQ software. Whether a 40 MHz or 80 MHz clock is used is determined by two types of wire bonding patterns of the hybrid.

Table 3.1: Hybrid Chip ID Address

Column 0		Column 1	
Chip Nr.	Address	Chip Nr.	Address
M 32	0100000	M 64	1000000
S 33	0100001	S 65	1000001
S 34	0100010	S 66	1000010
S 35	0100011	S 67	1000011
S 36	0100100	S 68	1000100
S 37	0100101	S 69	1000101
S 38	0100110	S 70	1000110
S 39	0100111	S 71	1000111
S 40	0101000	S 72	1001000
E 41	0101001	E 73	1001001

Figure 3.2 shows a hybrid test panel on an 8-way vacuum jig which hosts eight hybrids. The third position from the left side of the panel holds a working hybrid. In the first, fourth and last two positions from the left are hybrids without ASIC on them. The vacuum is used to suck down the hybrids to attach them flat and to improve cooling. The vacuum holes are visible on the rest of the three positions of the panel.

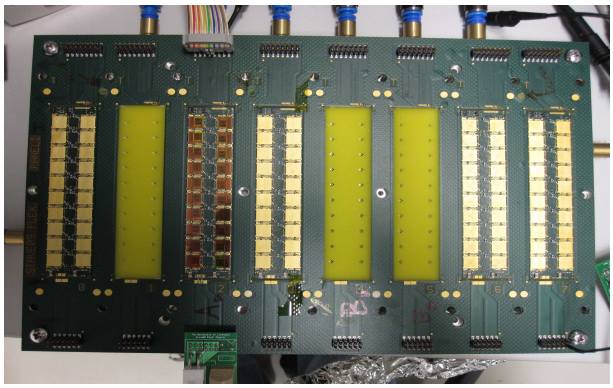


Figure 3.2: The Single Hybrid on a Test Panel

To test a single hybrid, a constant current of 4 to 4.5 A needs to be provided. The usual setting is 5V/4.5A in constant current (CC) mode, see Chapter 2.3.1.5. The actual output is around 3V/4.5A.

3.1.3 Dummy Module

A dummy module is a test module without a real silicon strip sensor attached. Instead of a real sensor, a copper sheet is used. As usual, the module contains two hybrids. Each hybrid has its own Buffer Control Chip (BCC), see Chapter 3.1.3.1. Figure 3.3 shows the dummy module which was used in the tests of the readout system.
To power the dummy module, a constant current of 4.5 A needs to be provided. The usual setting is 9V/4.5A with CC mode. The actual power drawn by the module is around 27 W (6V/4.5A).
The temperature of the dummy module on its own will rise to maximum of 90°C when it is powered. In order to make it work properly, cooling the module is necessary. Therefore the dummy module is placed on a testing jig which has a U-shaped cooling tube embedded and vacuum holes to fix the position of the module and to provide good thermal contact to the jig. A chiller flows the cooling fluid through the tube to transport the heat away which is generated during the test.

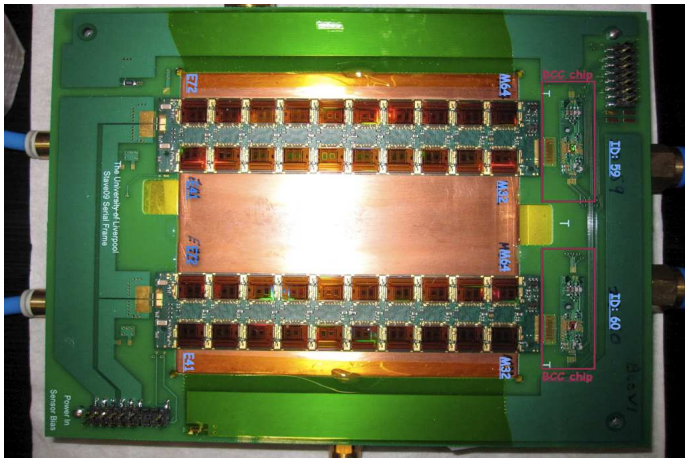


Figure 3.3: Dummy Module

3.1.3.1 BCC

Buffer Control Chip (BCC) is used to control the clock signal (both data clock and bunch crossing clock) of the module. With BCC board, there is no need to provide the data clock from HSIO which was necessary for the single hybrid testing. Instead of the data clock is derived from bunch crossing clock on the BCC chip itself.

3.2 DAQ System Setup

Figure 3.4 shows a schematic overview of the setup used at Zeuthen. The dummy module is tested in this case. The SCTupDAQ software is running on the DAQ PC to control and read out the module. It is connected through an ethernet cable to the HSIO and its interface board. The HSIO sends the commands and reads the data through a flat ribbon cable from the module. The HSIO is powered with 48 V from a commercial AC power supply unit. To test the dummy module, the cooling system (chiller and vacuum pump) is needed. For

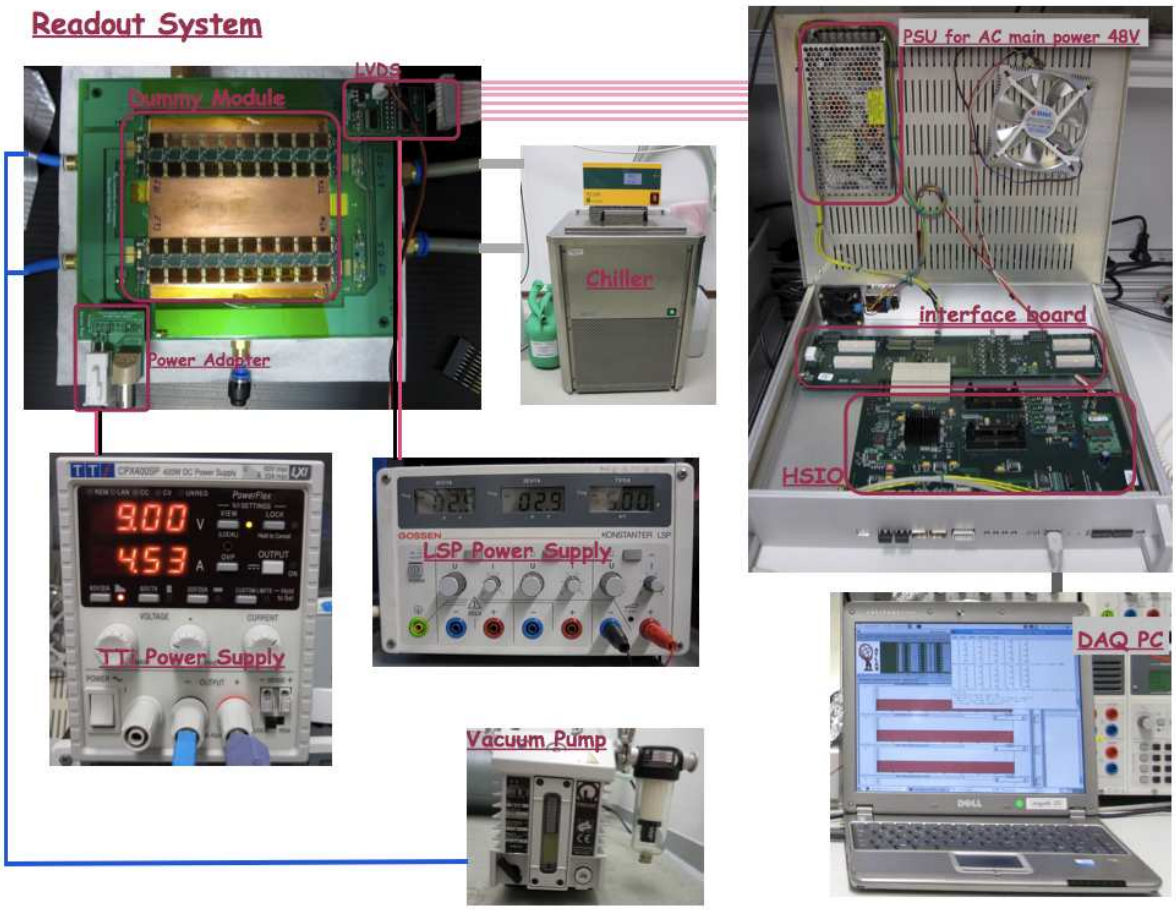


Figure 3.4: HSIO based readout system with Dummy Module

the temperature-varied tests, a nitrogen flow is provided to avoid reaching the dew point while testing at lower temperatures. Two power supplies (SP TTi CPX400SP and GOSSEN KONSTANTER LSP) separately power the dummy module and the LVDS buffer. The following section describes the details of the functions of each units.
Another high voltage power supply (Keithley 2410) will be used for depleting the sensor, when modules with real sensors are tested.

3.2.1 HSIO & Interface Board (RTM)

The HSIO board provides the signal processing capability. The interface board provides specific connectors and buffering which is required to interface with the front end detector electronics. Both of them are built in the Advanced Telecommunications Computing Architecture (ATCA) standard.

One of two connectors on the interface board, J37- and J38-IDC (Insulated Displacement Connector), establishes the communication with the device under test through a flat ribbon cable. The functions of the pinouts are listed in Table 3.2. The direct measurements of the signals (command, clock, etc.) can be done using a mixed signal oscilloscope. There are different pinout arrangements between single chip board (ABCN PCB PL1) and J37/J38 of the HSIO, details are shown in Table 3.2, too.

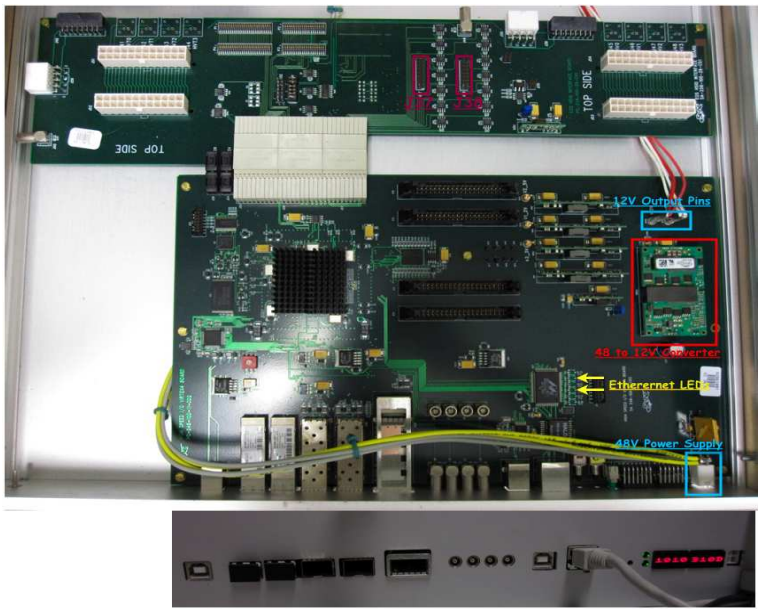


Figure 3.5: HSIO

Table 3.2: Pinout of HSIO J37 & J38 and ABCN PCB PL1

Pins	(1,2)	(3,4)	(5,6)	(7,8)	(9,10)	(11,12)	(13,14)	(15,16)
HSIO	Command	BCO	L1	DCLK	Data 1	Data 2	Reset	Ground
ABCN	Reset	Clock	Command	N/C	L1	N/C	Data Out	Ground

The DAQ PC controls signals and reads back the data from the HSIO through an ethernet cable. It is necessary to make sure the link is established correctly which is indicated by LEDs (100MBit transmitting and full duplex mode) before starting the test. See Figure 3.5 for the location of J37/J38 and the indicating LEDs.

The communication with the HSIO board is packet based. Packets are lists of command blocks which consist of opcodes and data. Opcodes initiate a dataless operation and data is written to a register. The packet is built in 16 bits structure. Register 9 controls the IDelay (stream delay). Register 16 controls the ABCN signals, like settings of command, clock, and pin assignments of the J37 or J38 connector. The settings for register 16 for the single chip board (Chip, 0×3801), single hybrid (Hybrid, 0×7883) and dummy module (Module, 0×1007 or 0×1047) are shown in Table 3.3. Register 23 mainly controls the 40/80 MHz data clock (DCLK) and have to be set to 0×40A0 (single chip board and single hybrid) or 0×00A0 (dummy module). The necessary register settings for configuring the different device under test are provided by special configuration and startup macros within the SCTDAQ software. Two 4 character display on the front panel of the HSIO board (right lower corner

Table 3.3: Register 16 of HSIO Data Format for ABCN Signals Control

Bit	Description	Chip 0×3801	Hybrid 0×7883	Module 0×1007	Module 0×1047
15	com shift 180	0	0	0	0
14	com shift 90	0	1	0	0
13	dclk enable	1	1	0	0
12	bco enable	1	1	1	1
11	invert reset	1	1	0	0
10	swap bco and dclk outputs	0	0	0	0
9	com into J38-IDC reset enable	0	0	0	0
8	com into J37-IDC reset enable	0	0	0	0
7	dclk invert	0	1	0	0
6	bco invert	0	0	0	1
5	com into J38-IDC L1 enable	0	0	0	0
4	com into J37-IDC L1 enable	0	0	0	0
3	com into stave L1R enable	0	0	0	0
2	stave com enable	0	0	1	1
1	J38-IDC com enable	0	1	1	1
0	J37-IDC com enable	1	1	1	1

of Figure 3.5) show the firmware version (eg. 1010 310D) when the HSIO is powered up and change to the bit address of Register 16 (eg. 1610 7883) after Register 16 is set.

3.2.2 LVDS Buffer Board

A Low-Voltage Differential Signaling (LVDS) buffer board is plugged onto the module side data cable connector. Signals are transmitted between the module and HSIO using 8 pairs of wires. See the details about the pinout in Table 3.2. LVDS implements the transmission of signals as the difference between the voltages on each wire of a cable pair in order to eliminate the disturbance of the noise and background.

3.3 Readout Tests – SCTDAQ

All the readout tests implemented in SCTDAQ software are used to achieve two main goals during module production: the characterization and confirmation of the module performance [10]. The test procedures can be separated into two parts. The first is to make sure the module being readout and configured correctly with several capture and burst scans. The second is to test the performance of the module with threshold scan based examinations. A performance test sequence usually is done in the follow order: 1.) Strobe Delay; 2.) 3 Point Gain (1fC/2fC); 3.) Trim Range; 4.) Response Curve; 5.) Noise Occupancy.

3.3.1 Capture Scan

3.3.1.1 Raw & Capture Burst

GOAL : To check the header and master chip assignment and chip IDs

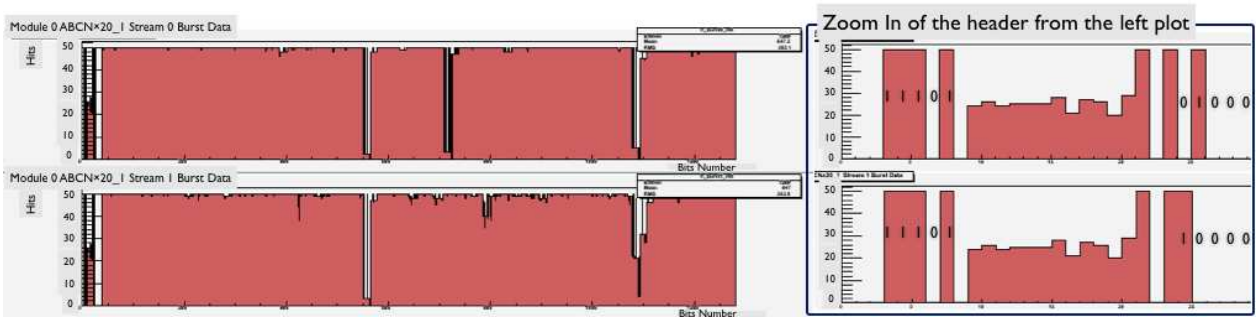


Figure 3.6: Raw Burst Histogram

Usually 50 triggers are sent by a Raw or Capture Burst test, of which the resulting stream of raw data return by the chips is plotted in a histogram. A Raw Burst will capture only events in which a header and trailer are found. A capture burst returns the raw bit patterns no matter if there was a header and trailer found. The left plots in Figure 3.6 show the raw data returned from two columns of a single hybrid, and the right plots are the zoom in of the headers from the left plots. The header contains the preamble (11101) in the beginning and the master chip address (M32, 0100000 and M64 1000000) at the end of the header. The x-axis shows the bit position, and y-axis is the summed up bit counts of the bit patterns returned for each of the 50 triggers.

3.3.1.2 ABCN Burst

GOAL : To check if the data from all chips can be decoded

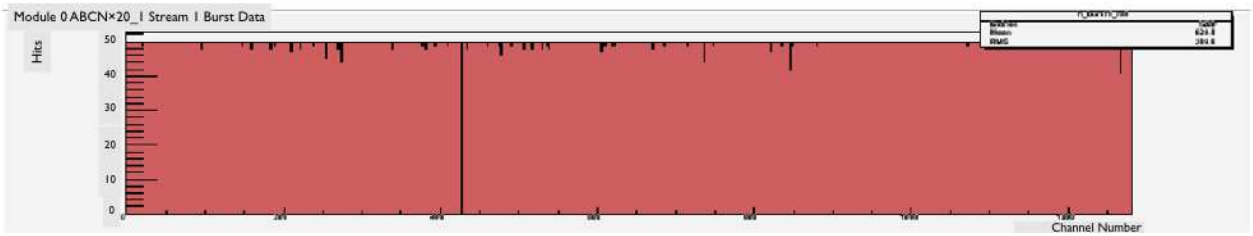


Figure 3.7: ABCN Burst Histogram

An ABCNBurst decodes the hit information, and plots channels which have hits. 50 triggers are sent and 50 hits per channel will be shown if the channel is activated and is working correctly. Figure 3.7 shows the hit information of the 1280 channels (=10 ABCN chips = 1 column) of a single hybrid.

3.3.1.3 Startup BCC

GOAL : To configure the BCC and to check the header and master chips IDs of modules using BCCs

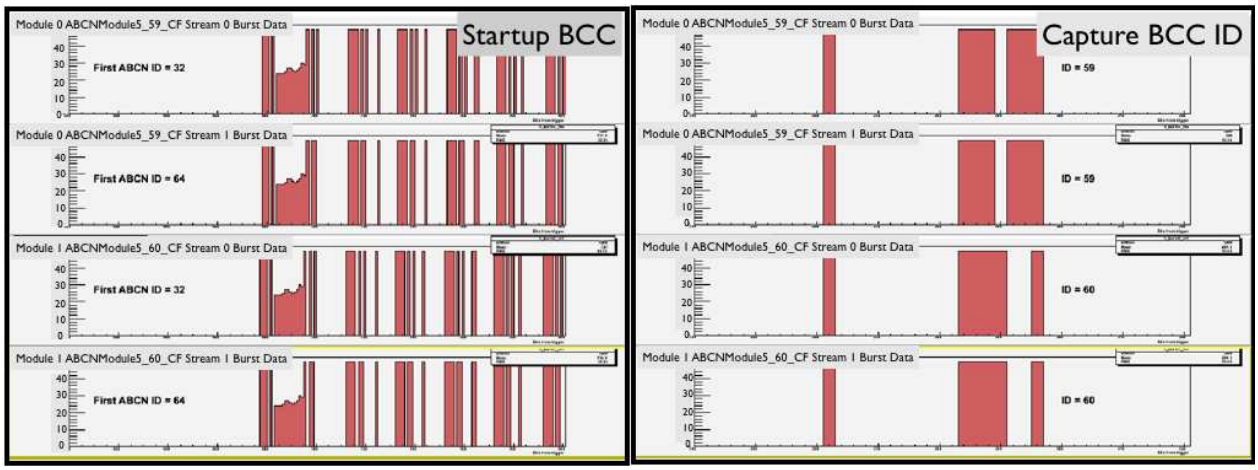


Figure 3.8: Startup BCC of Dummy Module

The Startup BCC macro is used to configure the BCCs and to check the correct function of the module after the BCC startup. The left plots of Figure 3.8 show the result of the Startup BCC function. The columns of hybrids sometimes flip in the wrong order (eg. 64, 32, 32, 64). The software needs to be restarted again to get the right order of the column ID.

3.3.1.4 Capture BCC ID

GOAL : To check BCC ID

It is also necessary to check that both columns of hybrid match the right BCC ID and make sure the configuration files are loaded correctly for each of the hybrids. The right plots of Figure 3.8 shows the result of the Capture BCC ID function. Compared with the Figure 3.3, both BCC ID 59 and 60 with two columns starting with M32 and M64 are readout correctly and using the corresponding configuration file (by checking the legends of the histograms).

3.3.1.5 IDelay Scan

GOAL : Adjust the sampling point for the returned data streams

The IDelay values should be set correctly in the configuration file in order to readout the module properly (especially for the full module). IDelay (or stream delay) values can be obtained by scanning through an internal delay within FPGA to accommodate for the phase shift in the clock signals of the data return by each column [43]. The delay values will change when different lengths of data cables and devices are used in the system.

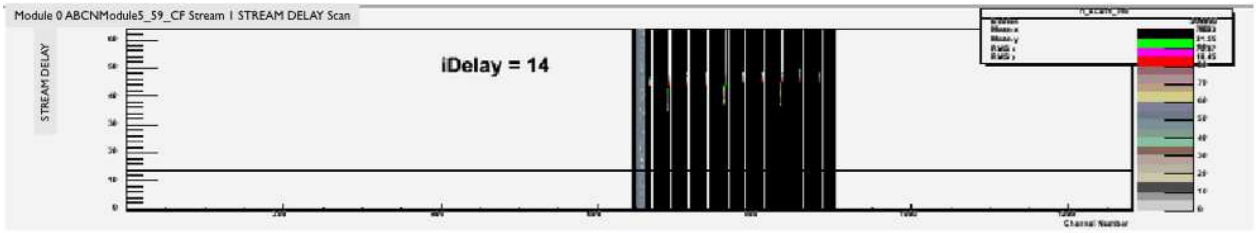


Figure 3.9: IDelay Scan

3.3.2 Strobe Delay

GOAL : To optimize the timing of the injected calibration charge

Test Procedure :

The injected charge is delayed by "a strobe". The propose of the delay is to make the injected charge being fired at the correct phase relative to the clock frequency. A 4 fC injected charge with 2 fC threshold is used in this test.

Performance Analysis :

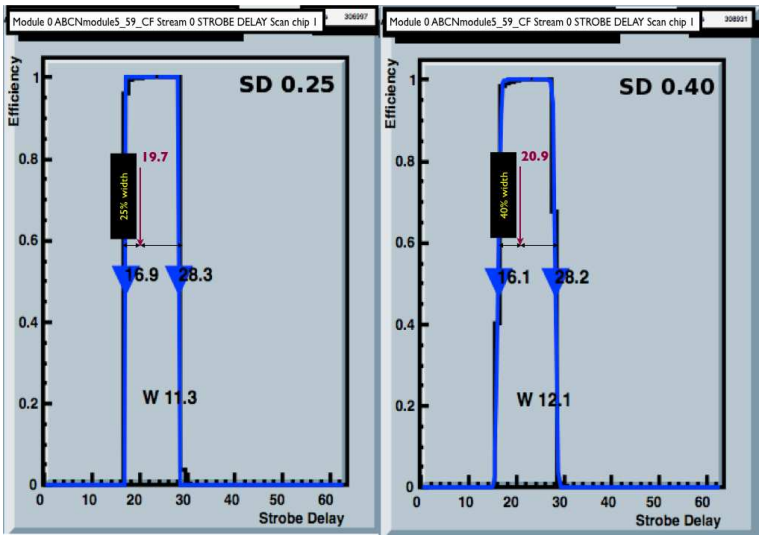


Figure 3.10: Strobe Delay Active Range

See the left plot of Figure 3.10. The x-axis shows 6 bit (0 to 63) DAC steps, each step corresponding to 0.8 ns in terms of the delay time. The y-axis is the hit efficiency (or hit probability over 200 hits). The left plot shows a range of delay time (16.9 DAC steps to 28.3 DAC steps) in which the injected charges are registered fully. For the Strobe Delay 0.25 test, the delay value is set at 25% of this active range and will be used for all the other following tests. In this example, the calibration strobe delay value is set at 19.7 DAC steps (15.76 ns). For the Strobe Delay 0.40 test, the value is set at 40% of the working range.

Test Result :

Strobe Delay 0.25

The strobe delay values will be set for each chip after the scan. The values will be applied for the following tests of the same measurement run. Figure 3.11 shows the plot of the scan results for one column of a module (or a hybrid). The x-axis represents the channel number, and the y-axis represents the strobe delay values (same as x-axis of Figure 3.10). The color of the plot shows the efficiency (hit probability).

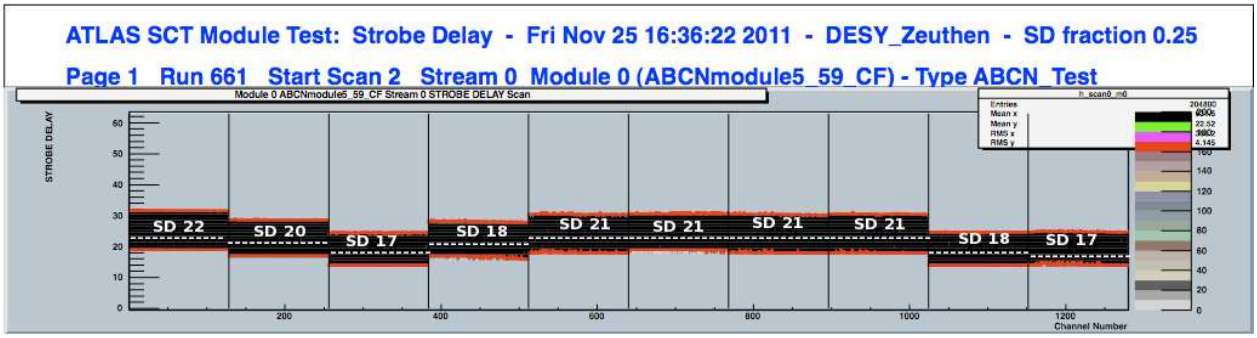


Figure 3.11: The Result of Strobe Delay 0.25 of Dummy Module

3.3.3 Gain Tests – 3 Point Gain & Response Curve

GOAL : To test the gain and noise performance of the device under test

Test Procedure :

Threshold Scan

The discriminator within the Front End block of ABCN25 readout chip maintain the hit which is registered from an event and discriminate the signal with a threshold, below the threshold returns "no hit" above the threshold returns "one hit".

With fixed value of injected charge, the test scans through difference threshold voltages for each readout channel. The hit probability decreases when the threshold voltage increases. For the ideal case, the injected charge results in a hit if it is above a certain threshold voltage and in no hit if below of the threshold. This threshold voltage (Vt50 point) is said to be the response value for the fixed injected charge.

Gain Tests

Different values of injected charges are used for the gain test. For each injected charge value a response value (Vt50) is obtained by a threshold scan. To observe the behavior over injected charge values versus their response (Vt50), the gain (or response curve) is obtained. The tests use different values of injected charge in the 3 Point Gain 1fC/2fC and Response Curve test, see Table 3.4. The Response Curve test is using ten different injected charge values and thus it can be seen as a 10 point gain test.

Table 3.4: Injected Charge of Gain Tests

	Injected Charge (fC)										fitting
3PT 1fC	0.52	–	1.00	–	1.48	–	–	–	–	–	linear
3PT 2fC	–	–	–	–	1.52	2.00	2.48	–	–	–	linear
RC	0.52	0.76	1.00	1.24	1.52	2.00	3.00	4.00	6.00	7.00	polynomial

S-Curve

S-Curve is the result plot of the threshold scan. In the ideal case, the result of a threshold scan should behave like a step function. Below a certain threshold the channel has 100% hit probability and above this certain threshold returns zero hit probability. But in reality, the threshold scan leads to a channel response shaped like a mirrored S in the presence of noise. The S-Curve can be fitted with the complementary error function, as shown in Figure 3.12. The complementary error function is the convolution of a step function and a Gaussian function. The Gaussian function curve can be interpreted as a function which expresses the noise, shown in Equ. 3.1 :

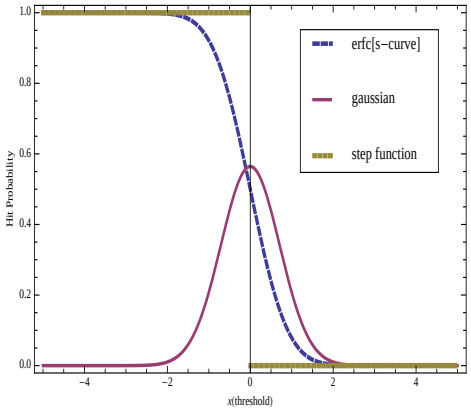


Figure 3.12: S-Curve

$$S(x) = \frac{1}{2}\mathrm{erfc}(x) = \frac{1}{2}(1 - \mathrm{erf}(x)) = \frac{1}{2} - \frac{1}{\sqrt{\pi}} \int e^{-x^2}\,\mathrm{d}x = \frac{1}{2} - \frac{1}{\sqrt{\pi}} \int G(x)\,\mathrm{d}x \tag{3.1}$$

By fitting the S-Curve of the threshold scan, x can be written as

$$x = \frac{\mathrm{Vt50} - \mu_s}{\sqrt{2}\sigma_s} \tag{3.2}$$

where μ_s is hit probability, σ_s is the Gaussian noise (named as "output noise" of SCTDAQ tests), and Vt50 is the threshold voltage at 50% hit probability.

Fitting Function of Response Curve

With different injected charges, the channels have different Vt50 values. The function of these in dependence of the injected charge is the response curve. With small injected charges (less than 2.5 fC), the response curves behave nearly linear. The gain is defined as the first derivative of the response curve. The software implements four different fitting functions of the response curve to analyze the results of the gain tests. For small injected charges, the gain is equal to the slope (p_1, the first derivative) of the response curve. When the injected charges increase above 2.5 fC, the non-linearity of the response curve (p_2, the deviation from the slope of small injected charges) is getting important. Therefore for the current analysis macros in SCTDAQ software, a linear fit is used for three point gain test (both 1fC and 2fC) and a polynomial fit is used for the ten point gain test (so called "response curve" in the software).

Table 3.5: Fitting Function of Response Curve

Linear Fit	$g = \frac{\mathrm{Vt50}_2 - \mathrm{Vt50}_1}{q_2 - q_2} = p_1$
Exponential Fit	$g = \frac{p_0 e^{-\frac{q}{p_1}}}{p_1\left(1+e^{-\frac{q}{p_1}}\right)^2}$
Grillo Function Fit	$g = \frac{p_1}{\left(1+\frac{p_1^2 q^2}{p_2^2}\right)^{\frac{3}{2}}}$
Polynomial Fit	$g = p_1 + 2p_2 q$

g, Gain (mV/fC)
q, Injected Charge (fC)
p_0, Offset (mV)
p_1, Small Signal Gain
p_2, measurement of the non-linearity

One example of polynomial fit of response curve of M32 in hybrid 59 of Dummy Module : with $q = 2$ fC, $p_0 = 30.53$, $p_1 = 112.15$, $p_2 = -1.53$; the gain is calculated as 106.08.

With the results of gain and the output noise (σ_s), the input noise (innse) is obtained :

$$\text{innse} = 6250 \times \frac{\sigma_s}{\text{gain}} \tag{3.3}$$

Test Result :

Response Curve

There are four result histograms of a Gain test generated, plotting the Vt50 points, the gain, the offset and the input noise over the 1280 channels of one column, as shown in the four left plots of Figure 3.13. The four plots on the right show curves of the response, the gain, the output noise and the input noise over ten (or three for the 3 Points Gain tests) injected charges.

The input noise is given in the unit of ENC (Equivalent Noise Charge) which is converted from fC to electrons by multiplying it by the number of electrons (6250) in 1 fC [45].

3.3.4 Trim Range

GOAL : To minimise the channel to channel variations of the threshold.

Test Procedure :

The threshold changes not only with respect to the injected charge but also the offset of the discriminator. The offsets vary from channel to channel and the spread will increase when the detectors accumulate radiation damage [11]. In order to keep the homogeneity of all channels, threshold correction is needed, which is performed during the trimming process of the Trim Range test.

Two main registers are used in the Trim Range test: TrimDAC (Trim Digital to Analog Converter) register and Mask register. The test procedure is first to check the initial Trim-

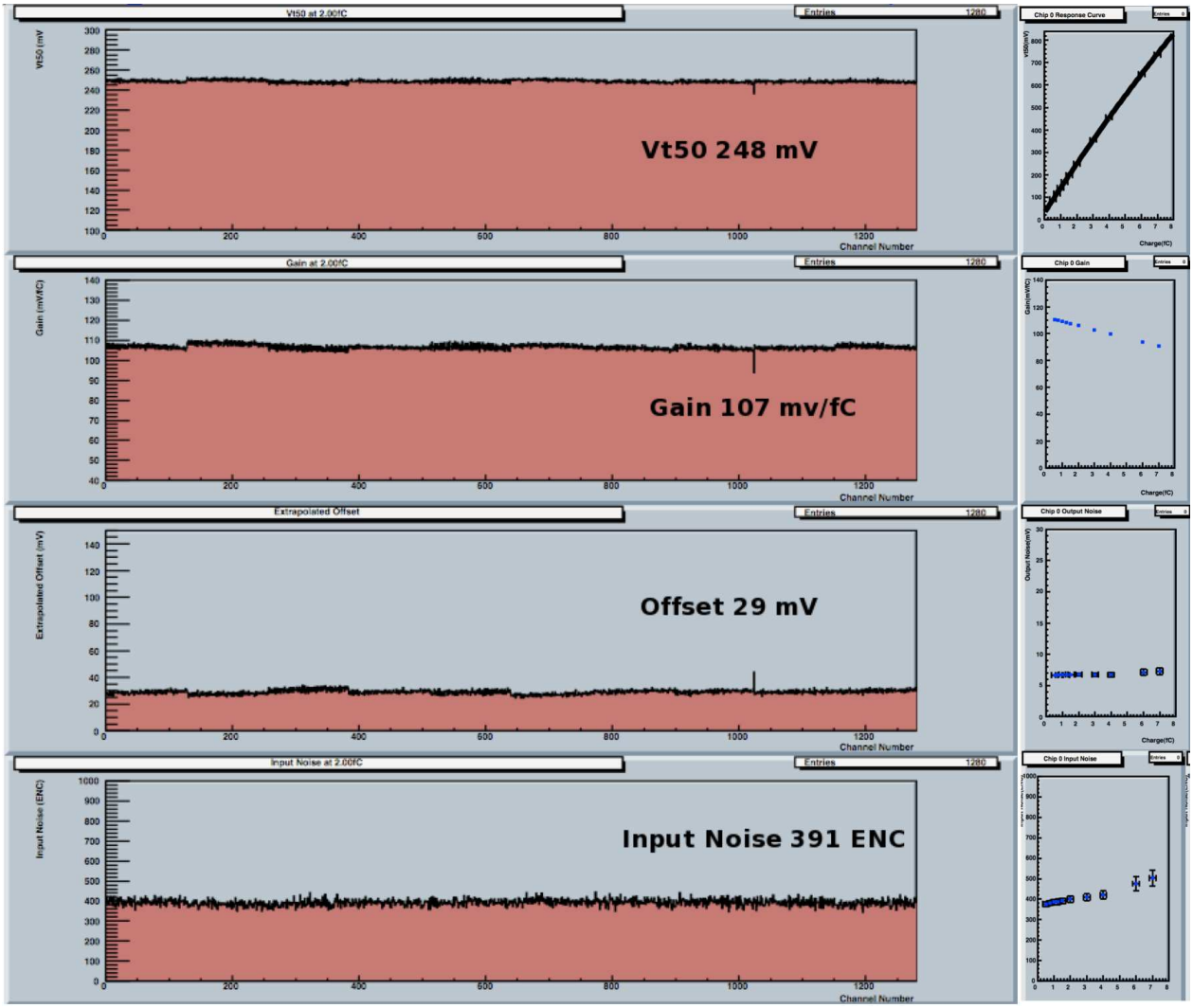


Figure 3.13: The Result of Response Curve of Dummy Module

DAC characteristic which is the confirmation of the linearity and uniformity of the TrimDAC curve (Figure 3.14). In the test 1fC charges are injected and the thresholds trimmed to the target values using eight different Trim Ranges. Each Trim Range set the range to trim the threshold with different trim steps.

Test Result :

Figure 3.14 shows the curve of trim range 0 result of chip M32 of the Dummy Module. There are eight curves within a figure, each curve represents how the threshold increases with respect to four different TrimDAC settings. These eight curves are with eight different threshold starting points (eg. from 128.0 mV to 172.8 mV). The slopes show how much the threshold changes with different TrimDAQ settings. The larger the TrimRange, the more the threshold is increased

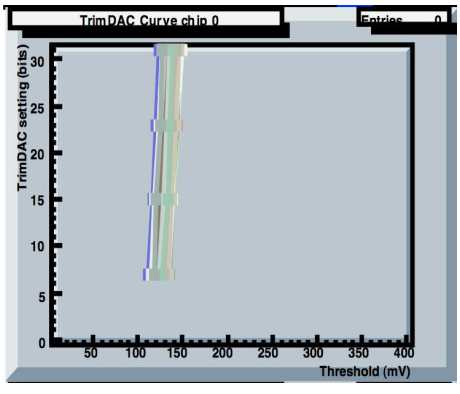


Figure 3.14: TrimDAC Curve

by trimming. The slopes with different Trim Range are shown in the rightmost plot of Figure 3.15.

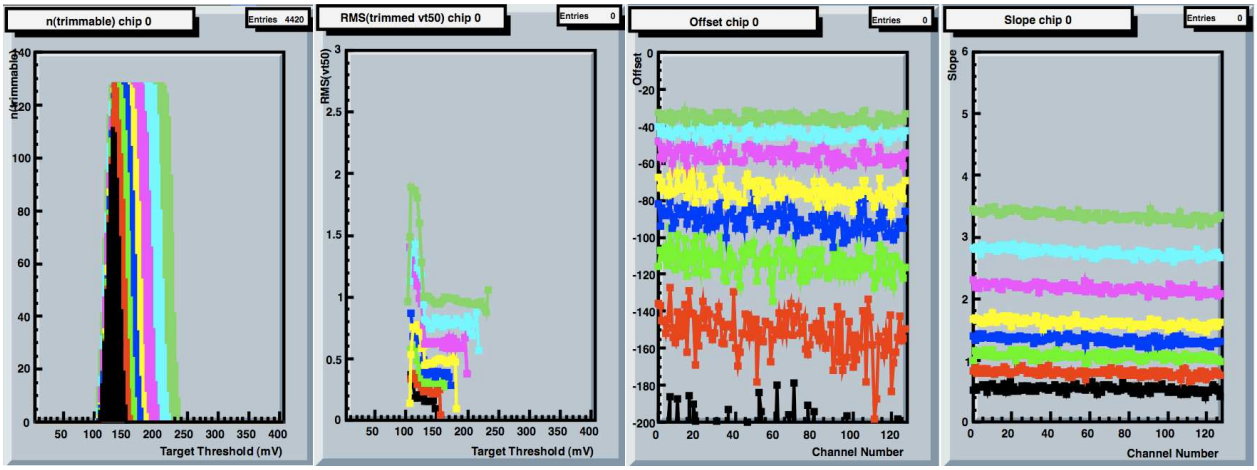


Figure 3.15: Trim Range Result

Each Trim Range has its target threshold to trim, the leftmost plot of Figure 3.15 shows the trimmable number of channels versus the target threshold. Eight different colors correspond to eight different Trim Ranges (black is Trim Range 0).

After eight full run of the Trim Range test, 9 ".trim" and 9 ".mask" files will be generated. Each Trim Range (from 0 to 7) has its corresponding ".trim" and ".mask" files. Another ".trim" and ".mask" file (defined its name with –1) will combines the best results from within the eight Trim Ranges and generates the trim and mask files to be loaded for another new test run without repeating the Trim Range test again. In the "–1" trim and mask files, each chip uses the most suitable Trim Range to be trimmed and masked and achieve the optimized target threshold.

In general, the smaller the Trim Range, the more channels are masked. The optimal concept is to use the smallest Trim Range possible without additional channels being masked. In the case of the Dummy Module, the Trim Range 2 and 3 are used the most in the optimized trim and mask files.

Figure 3.16 shows the result of a Reponse Curve before (the left plot) and after (the right plot) the Trim Range test. To evaluate how well the trimming went, the spread of Vt50 and the offset are two important criteria.

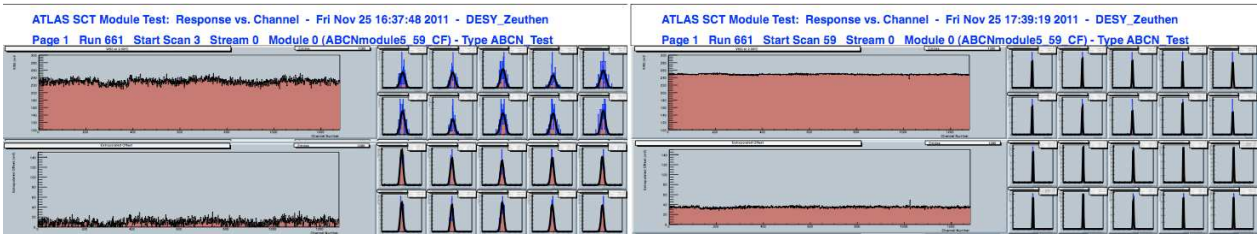


Figure 3.16: Trim Range Result

3.3.5 Noise Occupancy

GOAL : Direct measure of the noise present in a channel.

Test Procedure :

This test performs scans across the threshold without injecting any change. It provides a direct measure of the noise present in a channel. The threshold scan in this test is from -75mV to +75mV relative to the threshold voltage (Vt50) for 1 fC injected charge. Thresholds far below 0 mV (1fC level) return occupancies of 1, with the channel recoding the background noise. As the threshold increases, the number of noise hits reduces and to compensate, the number of triggers sent is increased from 2000 to 10^6.

Performance Analysis :

The probability p of surpassing a threshold V_{thr} is given by the complementary error function

$$p(V_{thr}) = \frac{1}{2}\mathrm{erfc}\left(\frac{V_{thr}}{\sqrt{2}}\right) \tag{3.4}$$

For thresholds much larger than the single channel random noise ($V_{thr} \gg 1$) this probability can be approximated by

$$\ln(p) \approx -\frac{1}{2}V_{thr}^2 - \ln\left(\sqrt{2\pi}V_{thr}\right) \tag{3.5}$$

Test Result :

There are three kinds of result plots obtained from this test.

Firstly, the right plot of Figure 3.17 shows the mean noise occupancy of all channels in a logarithmic scale versus the relative threshold . The left plot of Figure 3.17 shows the results of different channels (x-axis), here the y-axis is the threshold and the noise occupancy values are indicated by different colors.

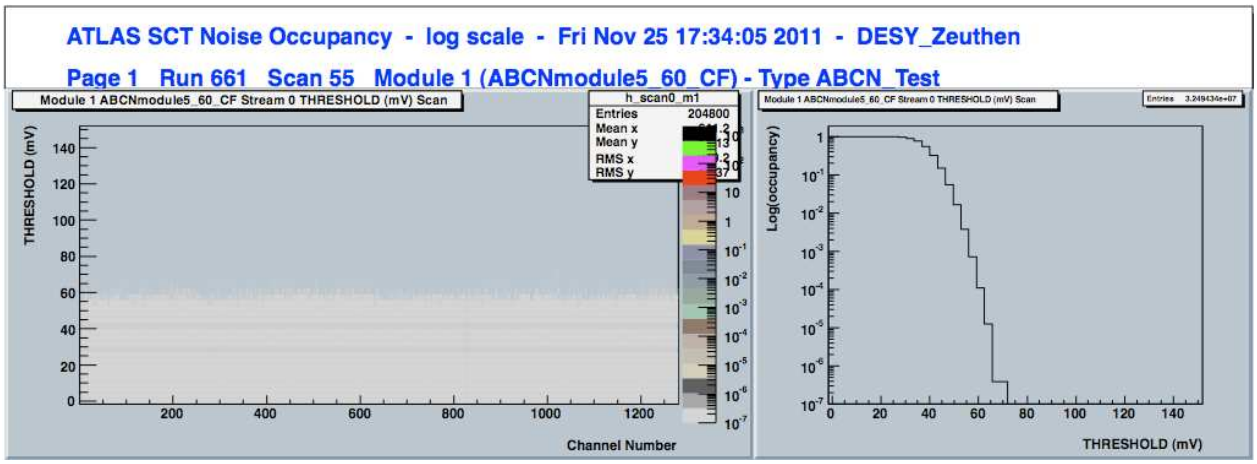


Figure 3.17: The Result of Noise Occupancy of Dummy Module

Secondly, the threshold square versus the log scale of the noise occupancy. According to the approximation (Equ. 3.5), we should get linear fit in this kind of plots, as shown in the left plot of Figure 3.18.

Thirdly, the s-curve of each chip with 4 different calibration lines. Each channel of the chips has an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The four calibration bus lines connect the calibration capacitors of every fourth channel. Every fourth channel can be tested simultaneously and get the strobe and address signals from the control circuity. For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitors via the input pads (CAL0, CAL1, CAL2, CAL3). Noise Occupancy tests these four calibration lines, and shows four resulting S-Curves of each chip. One of the results (CAL0) is shown in the right plot of Figure 3.18.

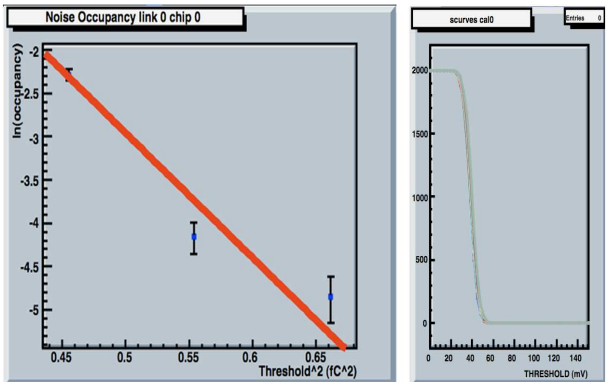


Figure 3.18: S-Curve Noise Occupancy of Dummy Module

3.4 Database Structure

In order to efficiently check the results of the testing and the quality of the future mass production of the modules, a database needs to be established. The original SCTDB (SCTDAQ DataBase) is modified to interface to the local database system at DESY Zeuthen (Zeuthen Measurement Database).

3.4.1 SCTDB

The information to confirm and to qualify the performance of the device under test should contain the test results in SCTDAQ (described in Chapter 3.3, but without the Burst results). Three different types of files will be generated after the full run of the tests.

3.4.1.1 File Types and Contents

First, the ".txt" files, show the general information of tests which include the test date, operator's name, the location, which kind of device under test, test name, test run number and the data of each test result. The test data of StrobeDelay contains the delay time of each chip. 3PointGain/ResponseCurve shows the results of q (Injected Charge), p_0 (Offset),p_1

(Small Signal Gain), p_2 (measurement of the non-linearity) and which fitting function was used. Also the Vt50, Gain, Offset, Input Noise and Output Noise of each chip are written in this result file. For the TrimRange test data, the target threshold, the number of trimmed channels are recorded for each eight Trim Ranges. The test data of NoiseOccupancy include the offset, mean and RMS (root mean square) occupancy.
Beside the general ".txt" result file, after the tests of 3PointGain/ResponseCurve, the raw data of every channel's gain, offset, and input noise are written into another text file. Also the comment of each channel will show. Several comments like "low gain" (the gain less than 75% of the chip mean gain value), "high gain" (the gain more than 125% of the chip mean gain value), "low offset" (less than chip mean offset –80), "high offset"(more than chip mean offset +80), "noisy" (input noise large than 115% of the chip mean value) are coded within the source code. In the case of testing of Dummy Module, the comments also recorded as "unbonded" (the readout channel does not attach to the sensor).
Second, the ".trim" and the ".mask" files are generated after TrimRange test. The detail of the files have been discussed in Chapter 3.3.4.
Third, the ".ps" (postscript) files shows all the histogram of each test. The "Test Result" plots of the Chapter 3.3 are examples of these histogram.

3.4.1.2 Upload

The SCTDB is designed to upload the files through a JAVA script, and to construct the database with Perl.

3.4.2 Zeuthen database

The Zeuthen Measurement Database is mainly developed and maintained by the IT department at DESY Zeuthen. It is a common project of the local ATLAS and CMS groups. The database system is mainly written and implemented in SQL (and Perl). The database system features a web interface.
The web application of the database provides access from almost everywhere and no need to install software for using the database. There are five major parts in the web front end: measurement, modification, simulations, shipments and some free action, as shown in Figure 3.19. The result text files are listed in the measurement subpage. For the corresponding ".ps", ".trim" and ".mask" can be attached to the result text file and listed in the same row. The core of the Zeuthen Database structure is "History". Each result file in the database should contain correct a "time stamp" (dd/mm/yyyy hr:min, eg. 09/12/2011 16:49) in the header to trace each measurement. Details of the database structure are shown in Figure 3.20.

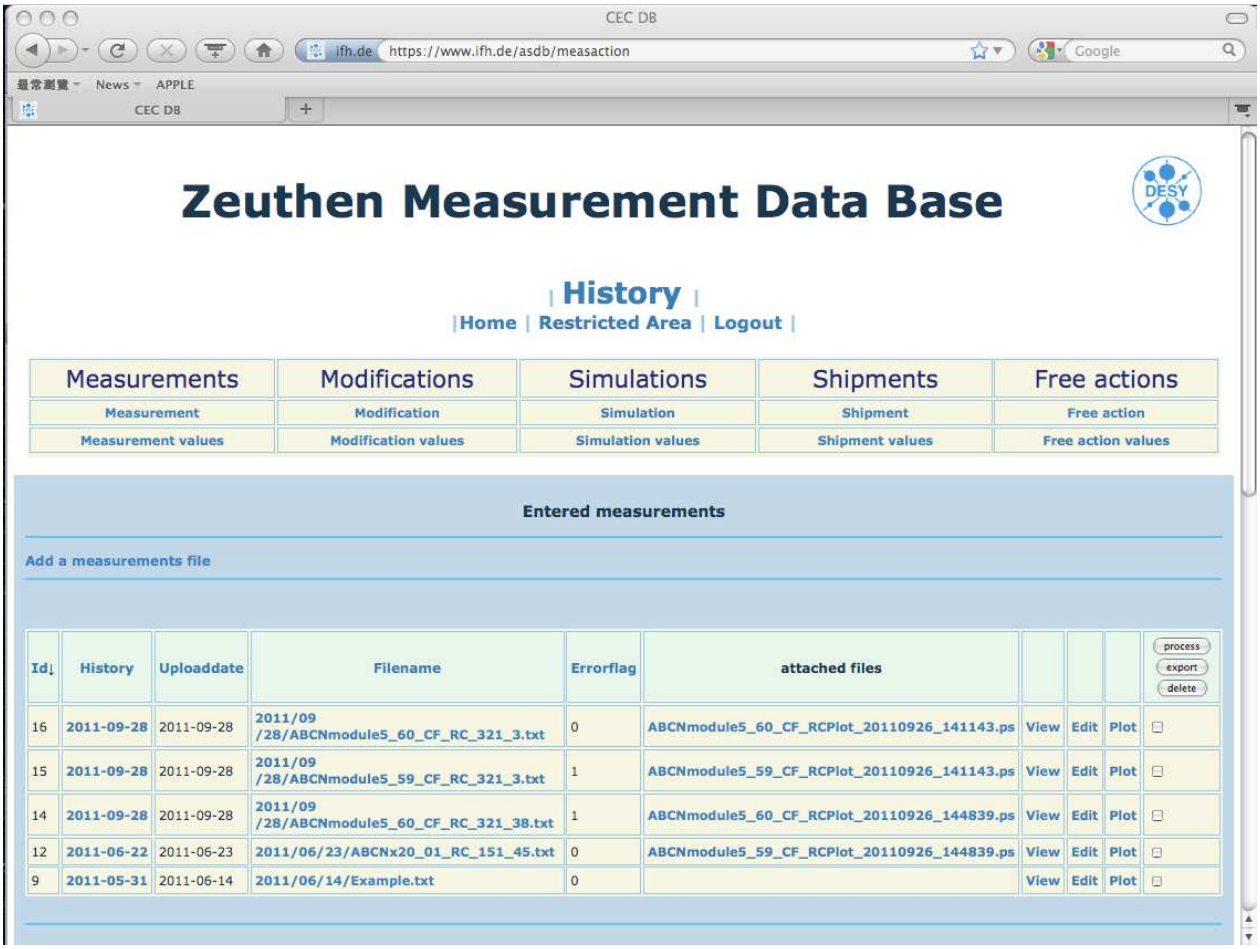


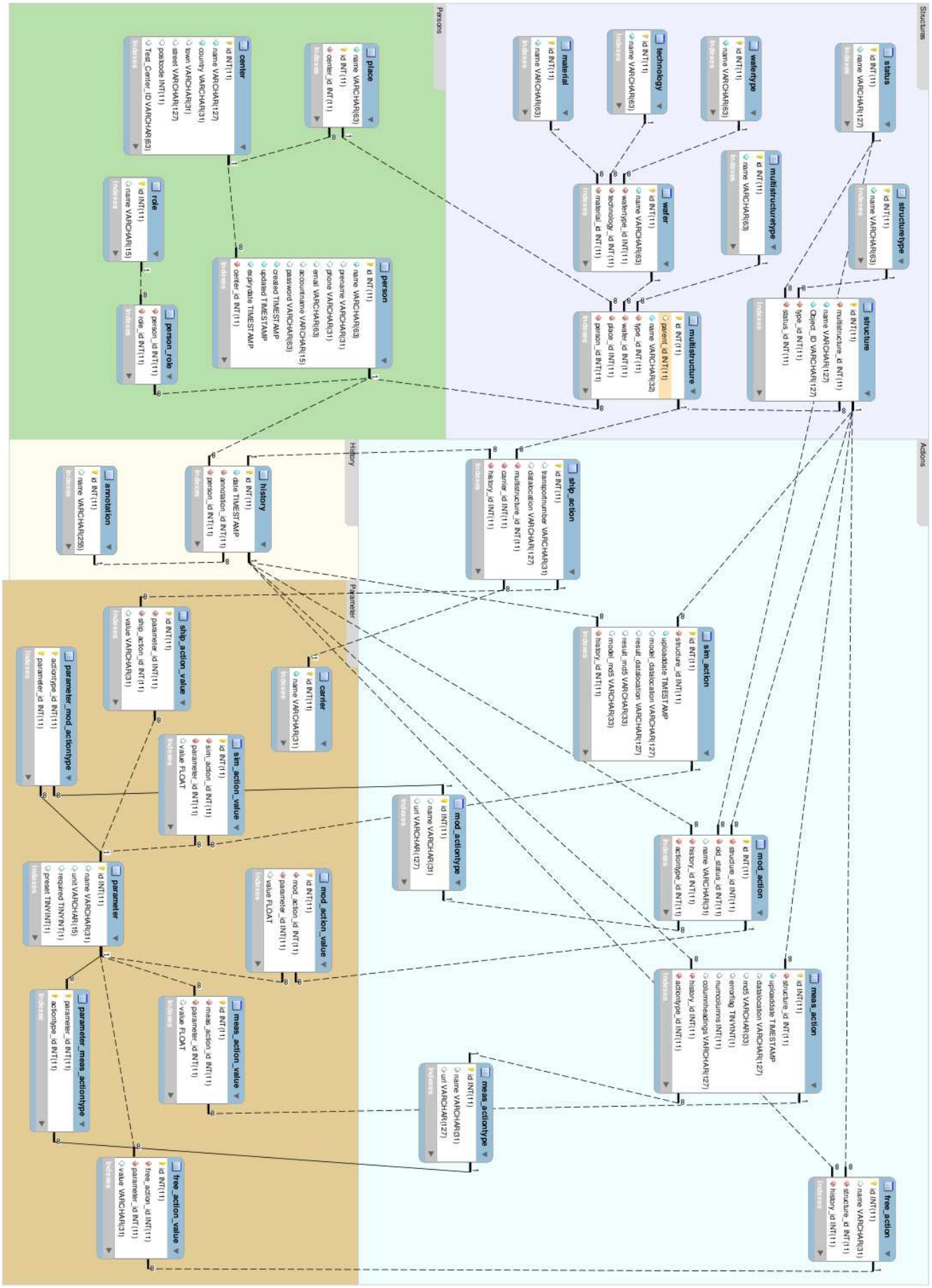
Figure 3.19: Screenshot of the Webpage of Zeuthen Database

3.4.2.1 Interface between SCTDB and Zeuthen DB

Due to the syntax difference between SCTDB and the Zeuthen Database, a Python script is written to harmonize the communication. The modification is to keep the original file which might be used for the original SCTDB and generate the new results for the Zeuthen Database.

3.4.2.2 Upload

All the results files can be uploaded either by the web interface or by running the Python script which specially coded for the SCTDAQ. The Zeuthen database website is user name and password specified. The upload via the Python script written by tokenizing the "cUrl" command line and getting the cookie from the web front end. Tokenizing the command is the way to harmonize the syntax to be used in Python. By entering the user name and password, "cUrl" can get the corresponding "cookie" to access the database and upload the target files.


Structures
Persons
Actions
History
Parameter
status
id INT(11)
name VARCHAR(127)
structuretype
id INT(11)
name VARCHAR(63)
waferype
id INT(11)
name VARCHAR(63)
multistructuretype
id INT(11)
name VARCHAR(63)
technology
id INT(11)
name VARCHAR(63)
material
id INT(11)
name VARCHAR(63)
wafer
id INT(11)
name VARCHAR(63)
waferype_id INT(11)
technology_id INT(11)
material_id INT(11)
structure
id INT(11)
multistructure_id INT(11)
name VARCHAR(127)
Object_ID VARCHAR(127)
type_id INT(11)
status_id INT(11)
multistructure
id INT(11)
parent_id INT(11)
name VARCHAR(32)
type_id INT(11)
wafer_id INT(11)
place_id INT(11)
person_id INT(11)
place
name VARCHAR(63)
id INT(11)
center_id INT(11)
center
id INT(11)
name VARCHAR(127)
country VARCHAR(31)
town VARCHAR(31)
street VARCHAR(127)
postcode INT(11)
Test_Center_ID VARCHAR(63)
person
id INT(11)
name VARCHAR(63)
prename VARCHAR(31)
email VARCHAR(63)
accountname VARCHAR(15)
password VARCHAR(63)
created TIMESTAMP
updated TIMESTAMP
expirydate TIMESTAMP
center_id INT(11)
role
id INT(11)
name VARCHAR(15)
person_role
person_id INT(11)
role_id INT(11)
ship_action
id INT(11)
transportnumber VARCHAR(31)
datalocation VARCHAR(127)
multistructure_id INT(11)
carrier_id INT(11)
history_id INT(11)
sim_action
id INT(11)
uploaddate TIMESTAMP
model_datalocation VARCHAR(127)
result_datalocation VARCHAR(127)
result_md5 VARCHAR(33)
model_md5 VARCHAR(33)
history_id INT(11)
mod_action
id INT(11)
structure_id INT(11)
sql_status_id INT(11)
name VARCHAR(31)
history_id INT(11)
actiontype_id INT(11)
meas_action
id INT(11)
structure_id INT(11)
uploaddate TIMESTAMP
datalocation VARCHAR(127)
md5 VARCHAR(33)
errorflag TINYINT(1)
numcolumns INT(11)
columnheadings VARCHAR(127)
history_id INT(11)
actiontype_id INT(11)
free_action
id INT(11)
name VARCHAR(31)
structure_id INT(11)
history_id INT(11)
history
id INT(11)
date TIMESTAMP
annotation_id INT(11)
person_id INT(11)
annotation
id INT(11)
name VARCHAR(255)
carrier
id INT(11)
name VARCHAR(31)
ship_action_value
id INT(11)
parameter_id INT(11)
ship_action_id INT(11)
value VARCHAR(31)
sim_action_value
id INT(11)
sim_action_id INT(11)
parameter_id INT(11)
value FLOAT
mod_actiontype
id INT(11)
name VARCHAR(31)
url VARCHAR(127)
mod_action_value
id INT(11)
mod_action_id INT(11)
parameter_id INT(11)
value FLOAT
meas_actiontype
id INT(11)
name VARCHAR(31)
url VARCHAR(127)
meas_action_value
id INT(11)
meas_action_id INT(11)
parameter_id INT(11)
value FLOAT
free_action_value
id INT(11)
free_action_id INT(11)
parameter_id INT(11)
value VARCHAR(31)
parameter
id INT(11)
name VARCHAR(31)
unit VARCHAR(15)
request TINYINT(1)
preset TINYINT(1)
parameter_mod_actiontype
parameter_id INT(11)
actiontype_id INT(11)
parameter_meas_actiontype
parameter_id INT(11)
actiontype_id INT(11)

Chapter 4

Systematic Study of DAQ Readout System

In order to make the DAQ readout system stable and less noise, the study about how to improve and optimize the setup is described in this chapter. LVDS buffer board is provide the function to double the signals and reduce the noise. To check the clock signals with different devices under test with or without the LVDS buffer board helps us to understand how the electromagnetic interference could disturb the signals. And the study of bunch crossing clock and data clock signals can show the function of BCC. This chapter also describes the noise performance in two difference cases.

4.1 Clock Signal

Clock signals behave differently with different device under test being read out. The main difference is the BCC chips. Table 4.1 presents the bunch crossing clock (BCO) and data clock (DCLK) signals during the readout. Clock signals are managed by two pairs of pinouts, details see the Table 3.2. To measure the clock signals, pin 4 (BCO) and pin 8 (DCLK) are attached to the mixed signal oscilloscope separately. The ideal way to measure the signals is to attach a pair of the pins (e.g. pin 4 and pin 5 for the BCO) with oscilloscope. But due to a technical problem, the results presented here are only with one pin attached which means there is some information loss about the function of LVDS buffer board.
Table 4.1 gives the measurement results of the clock signal period (eg. 25 ns), the amplitude of the signals (amp.) and the baseline of the waveform. Signals will become stronger when the hybrids/modules are powered. For the Dummy Module, the data clock is generated by the BCC chips, therefore there is no data clock sent during the readout.

	BCO (pin 4)	DCLK (pin 8)
Single Hybrid without LVDS buffer board, hybrid without powering	25 ns, amp.:180 mV, baseline: 1.03 V	no signal
		after set reg. 16 to 7883: 25 ns, amp.:180 mV, baseline 1.03 V
Single Hybrid without LVDS buffer board, hybrid powered with TTi power supply	25 ns, amp.:221 mV, baseline: 1.19 V	no signal
		after set reg. 16 to 7883: 25 ns, amp.:260 mV, baseline 1.15 V
Single Hybrid with LVDS	with signal *	with signal *
Dummy Module with LVDS buffer board	25 ns, amp.: 419 mV, baseline: 1.43 V	no signal
	no signal when the power cycle of "Startup BCC v1" (reg. 16 set to be 0000)	

Table 4.1: The measurement results (the clock period, amplitude and baseline voltage) of two clock signals with two devices under test.
* the same result as the one without LVDS buffer board, but hybrid are not able to be readout when LVDS buffer board attached

4.2 Electromagnetic Interference

The stability of the readout system can be broken by the Electromagnetic Interference (EMI). Powering on and off electrical devices in the same electric circuit as the measurement setup can easily get the readout stuck or crash. The usual error messages after crash shown in the readout console are "Decoder error" or "Error packet in bitstream". If the readout get stuck, it usually does as at the status message "HSIO write reg 0 f".
One of the electromagnetic interference event generated by vacuum pump gave a pulse of several Volts as seen in the oscilloscope. This pulse disturbed the clock signal which is around hundred millivolt, see the Table 4.1.
To put the readout devices (HSIO, power supplies) and high power consumption device (chiller, vacuum pump) in the isolated circuitry helps reducing these the issues.

4.3 Noise Hunting

The noise of the readout system and the device under test depends on the operation temperature, stability of the system and plenty of the environment factors. Even if the same setup is used and with the same configuration parameters, the noise values still changed by some undiscovered environment factors. The following section discusses the trend of noise variation in two different cases.

4.3.1 Noise of Different Injected Charges

We observe in the test that the input noise values change with different injected charges. The results of Table 4.2 were repeated three times each after trimming in the same run of Dummy Module testing. With different run of the tests the noise varied around ± 20 ENC, but the trends are the same. The noise values behave as 1fC∼2fC<ResponseCurve.

Table 4.2: Noise of 3PointGain and Response Curve

	m59 (ENC)	m60 (ENC)
3PointGain 1fC	365 ± 20	373 ± 21
3PointGain 2fC	367 ± 21	378 ± 22
Response Curve	371 ± 18	383 ± 18

The mean values (μ) and their standard deviation (s) are calculate with the population-based statistics:

$$\mu = \frac{\sum_i n_i \mu_i}{\sum_i n_i} \tag{4.1}$$

$$s = \sqrt{\frac{\sum_i n_i s_i^2}{\sum_i n_i} + \frac{\sum_{i<j} n_i n_j (\mu_i - \mu_j)^2}{(\sum_i n_i)^2}} \tag{4.2}$$

The difference between the 3PointGain and Response Curve are the injected charges and the fitting function of Gain. The Input noise is computed from the output noise and the Gain, as shown in Eqn. 3.3. One of these two factors might be the reason cause the increase of the noise of the Response Curve results, but there is not yet a conclusive answer now.

4.3.2 Noise of Different Way to Power the HSIO Board

Powering up the HSIO board directly with a 12 V linear supply, which is originally used to power the fan for the cooling of 48 to 12 V converter, was tested to reduce the noise at the other sites of SCT community [46]. The layout of the 12 V linear supply and the converter are shown in Figure 3.5. But the results can not be repeated at Zeuthen.

Table 4.3: Noise of Different Way to Power the HSIO

	m59 (3PT 1fC)	m59 (3PT 2fC)	m60 (3PT 1fC)	m60 (3PT 2fC)
48 V	401 ± 21	449 ± 27	403 ± 29	453 ± 33
12 V	412 ± 25	464 ± 29	409 ± 29	464 ± 67

The input noise results of powering up with 48 V (original, the commercial AC power supply unit) and with 12 V output pins shows in Table 4.3. The unit of the input noise is ENC. 3PT is the abbreviation of 3 Point Gain tests. Each test set was done with the same run and repeated twice after trimming on the same day. Powering up the HSIO board of 12 V linear

supply consistently shows the higher noise. To compare the results of Table 4.2, it shows even if with the same setup, the noise values varied in the different test date.

Chapter 5

Summary and Conclusions

The scientific purpose of the LHC and the ATLAS experiment is to answer the fundamental open questions nowadays in physics.
The LHC collides two bunch of protons and the produced particles are detected by the ATLAS detectors. Each sub detectors of ATLAS manage different functionality of detection. In order to reduce the statistical uncertainties for measurements of rare process, higher luminosity of LHC is needed. To cope with the higher luminosity LHC, upgrade of the ATLAS detector are planned. The design of upgrade of detectors is to overcome two challenges : piles-up events and radiation damage. DESY focuses on the upgrade of end-caps of the ATLAS silicon strip detector: module production and testing.
The HSIO based readout DAQ system is used at DESY (Zeuthen site). Readout tests of SCTDAQ are performed to confirm and calibrate the module performance in preparation for future module production. In this thesis the test routines in the data acquisition software SCTDAQ were evaluated and the results were studied to achieve the goal of stable and noise-reduced readout system. A local database system was established to record the information for the future mass production.
In this thesis the readout system was tested in detail with several test devices, a single chip board, a single hybrid and a dummy module. The knowledge of the test results is used to optimize the readout system performance. The prototype of the Zeuthen database system interfaced to SCTDAQ is established. The instability of the readout system and noise performance are getting significant improved. The electromagnetic interference is the main source to cause the instability of system by studying the clock signals during the disturbs. The input noise results of ResponseCurve test are higher than 3PointGain test. The other noise source could also be related to the way to power the readout system.

Acronym List

General

- **ATLAS** A Toroidal LHC ApparatuS
- **CMS** Compact Muon Solenoid
- **DAQ** Data Acquisition
- **TDAQ** Trigger and Data Acquisition
- **ROD** Read Out Driver
- **TTC** Timing, Trigger, and Control
- **TIM** TTC Interface Module
- **ID** Inner Detector
- **SCT** Semiconductor Tracker
- **MCC** Module Controller Chip
- **FE** Front End
- **IP** Interaction Point, the place where particles collide (vertex)
- **IBL** The Insertable Beampipe Layer
- **ABCN** ATLAS Binary Chip - Next
- **SM** Standard Model
- **L1A** Level 1 Accept trigger

Hardware

- **SRAM** Static Random Access Memory, c.f. DRAM
- **LVDS** Low-Voltage Differential Signaling
- **HSIO** High Speed Input/Output
- **EUDET** Detect R&D towards the international linear collider
- **ASIC** Application Specific IC
- **FPGA** Field Programmable Gate Array
- **Virtex** a company producing FPGA
- **ATCA** Advanced Telecommunications Computing Architecture
- **ESD** ElectroStatic Discharge
- **PCB** Printed Circuit Board
- **RTM** Rear Transition Model
- **RCE** Reconfigurable Cluster Element
- **CIM** Cluster Interconnect Module
- **TRT** Transition Radiation Tracker

- **GPIB** General Purpose Interface Bus (IEEE-488)
- **ToT** Time over Threshold
- **IF** Interference Feedback
- **CMOS** Complementary Metal Oxide Semiconductor
- **W/L** the width to length ratio
- **VDDREF** reference voltage
- **DUT** Device Under Test
- **DAC** digital-analog converter
- **ADC** analog-digital converter
- **PROM** Programmable Read-Only Memory
- **VHDL** Very high speed integrated circuit Hardware Description Language
- **VHDL-AMS** Analogue Mixed Signal
- **FIFO** First In, First Out
- **DDL** Dynamic Link Library
- **CLOAC** CLOck And Control
- **MuSTARD** Multichannel semiconductor Tracker ABC(D) Readout Device
- **SLOG** SLOw command Generator
- **NIVXI** National Instruments VME eXtensions for Instrumentation
- **VCSEL** Vertical Cavity Surface Emitting Laser
- **DCS** Detector Control System
- **ENC** Equivalent Noise Charge
- **MVC** Model View Controller
- **SEU** Single Event Upsets
- **EMI** Electromagnetic Interference
- **VME** VERSAmodule Eurocard, a computer bus standard

SCTDAQ

- **cb** control blocks
- **CTB** Combined Test Beam

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